ISSN: 2454-9940

# INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

E-Mail :
editor.ijasem@gmail.com
editor@ijasem.org

www.ijasem.org

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024

# DESIGN OF HIGHTHROUGHPUT BASED MEMORY SYSTEM COMPRESSED BY USING FFT TECHNIQUE FOR HIGHSPEED COMMUNICATION SYSTEM

[1] NAMBURI NAGA SRIDEVI, [2]K RAGHU

**ABSTRACT:**
A high-throughput programmable fast Fourier transform (FFT) processor is designed supporting 16- to 4096-point FFTs and 12- to 2400-point discrete Fourier transforms (DFTs) for 4G, wireless local area network, and future 5G. A 16-path data parallel memory-based architecture is selected as a tradeoff between throughput and cost. To implement a hardware-efficient high-speed processor, several improvements are provided. To maximally reuse the hardware resource, a reconfigurable butterfly unit is proposed to support computing including eight radix-2 in parallel, four radix-3/4 in parallel, two radix-5/8 in parallel, and a radix-16 in one clock cycle. Twiddle factor multipliers using different schemes are optimized and compared, wherein modified coordinate rotation digital computer scheme is finally implemented to minimize the hardware cost while supporting both FFTs and DFTs. An optimized conflict-free data access scheme is also proposed to support multiple butterflies at any radices. The processor is designed as a general IP and can be implemented using a processor synthesizer (applicationspecific instruction-set processor designer).The fast Fourier transform (FFT) is a commonly used algorithm in digital signal processing areas, such as imaging applications and communication systems. Image processing requires computation sizes as high as 222.

## INTRODUCTION

Most embedded systems need to be self-reliant. It's not usually possible to wait for someone to reboot them if the software hangs. Some embedded designs, such as space probes, are simply not accessible to human operators. If their software ever hangs, such systems are permanently disabled. In other cases, the speed with which a human operator might reset the system would be too slow to meet the uptime requirements of the product. A watchdog timer is a piece of hardware that can be used to automatically detect software anomalies and reset the processor if any occur. Generally speaking, a watchdog timer is based on a counter that counts down from some initial value to zero. The embedded software selects the counter's initial value and periodically restarts it. If the counter ever reaches zero before the software restarts it, the software is presumed to be malfunctioning and the processor's reset signal is asserted. The processor (and the embedded software it’s running) will be restarted as if a human operator had cycled the power. The process of restarting the watchdog timer's counter is sometimes called "kicking the dog." The appropriate visual metaphor is that of a man being attacked by a vicious

[1]M.TECH VLSI, DEPT OF E.C.E, INTERNATIONAL SCHOOL OF TECHNOLOGY AND SCIENCE FOR WOMEN ANDHRAPRADESH,INDIA,533294

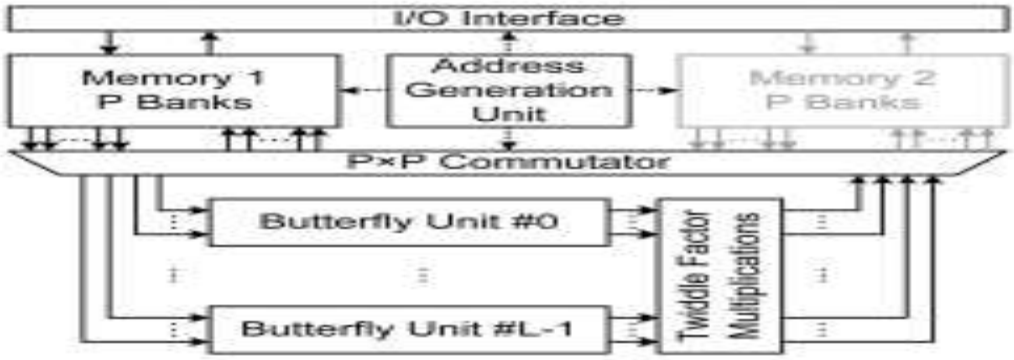
[2]ASSISTANT PROFESSOR,INTERNATIONAL SCHOOL OF TECHNOLOGY AND SCIENCE FOR WOMEN ,ANDHRAPRADESH,INDIA,533294

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024

dog. If he keeps kicking the dog, it can't ever bite him. But he must keep kicking the dog at regular intervals to avoid a bite. Similarly, the software must restart the watchdog timer at a regular rate, or risk being restarted. Watchdog timers may also trigger control systems to move into a safety state, such as turning off motors, high-voltage electrical outputs, and other potentially dangerous subsystems until the fault is cleared. For example, a watchdog timer can be implemented with a x-bit counter in a system working with a clock signal of y MHz, therefore, the system will shut down if the timer is not reset in a period of seconds. Watch dog timers have got various important applications one of them being in ATMs which we have studied and designed in our project.

EXISTING SYSTEM:

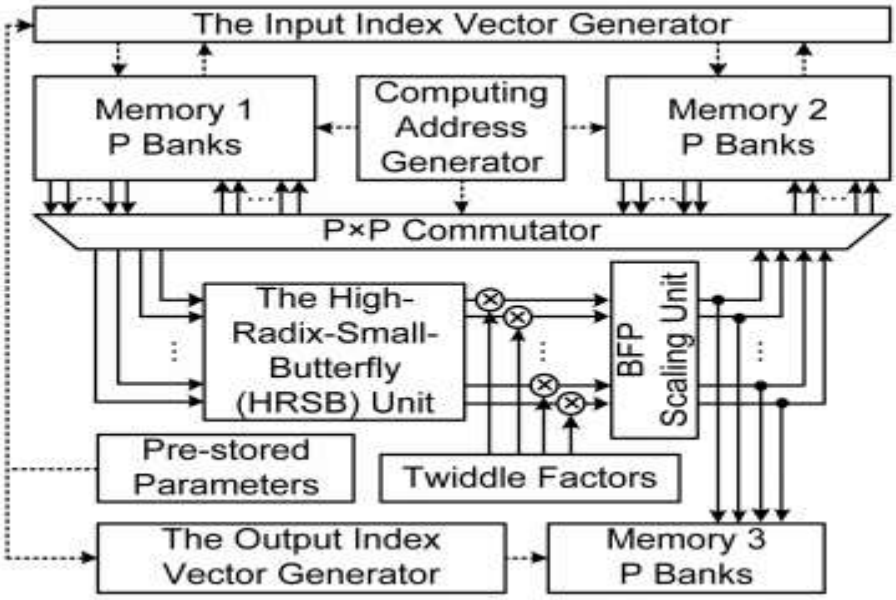
Memory-based FFTs usually include three stages: the input sampling, intermediate computations, and the output reordering. The continuous-flow mode should be available only if the computation time is not longer than the input/output time. Fig. 1 is a typical parallel-PE memory-based FFT adopting the in-place strategy, which consists of L parallel radix-r PEs and two P-bank memory groups. Consequently, the continuous- flow memory-based FFT should satisfy $Nr \,.\, L \,.\lceil \log_r N \rceil \leq N$ where $\lceil \log_r N \rceil$ is the recursive computation stages. The total number of parallel paths of the PEs is $P = r \cdot L$. As a result, increasing the radix r or the PE parallelism L represents two basic methods of satisfying (1).




Architecture of a multiple-PE, memory-based FFT processor.

PROPOSED SYSTEM: There are two different FFT modules in LTE system: one is the $2_n$ mode ($n$ = 7–11) FFT, and the other is the 35 different-length NSPP DFT, whose transform sizes range from 12 to 1296.

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024




Block diagram of the proposed FFT processor architecture.

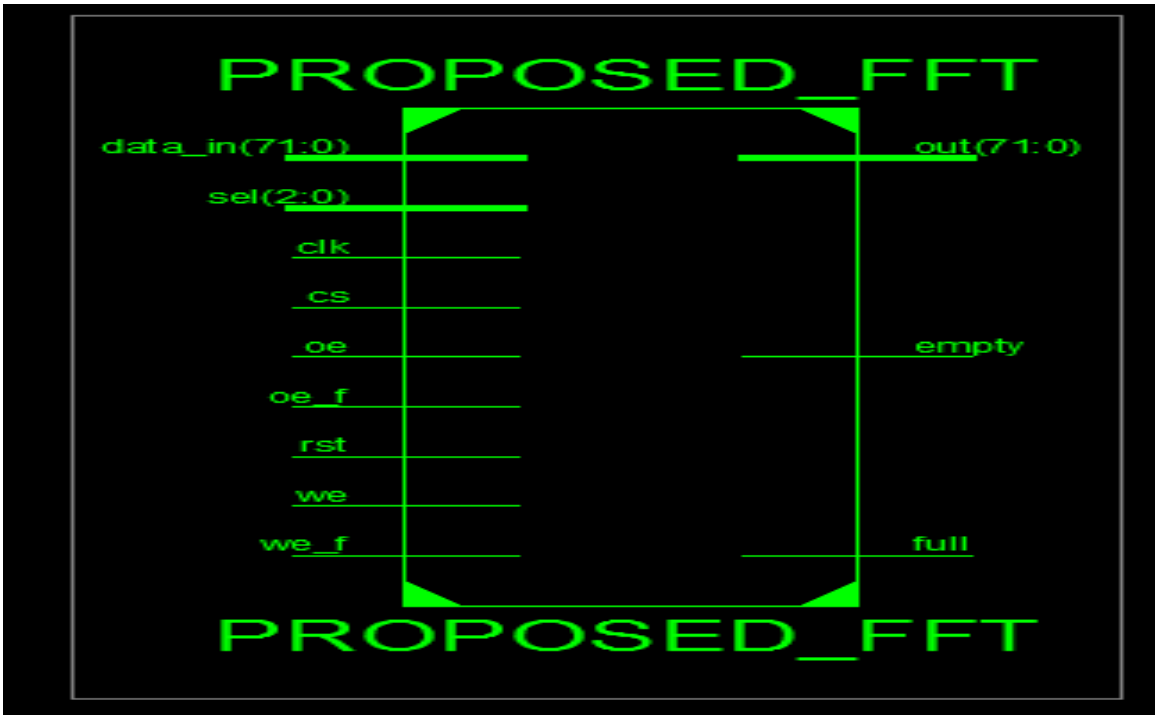
FAST Fourier transform (FFT) is a compute-intensive algorithm in the physical layer of an orthogonal frequencydivision multiplexing (OFDM) system to convert data between time domain and frequency domain. Many OFDM systems such as 4G LTE/LTE-A [1] and wireless local area network (WLAN) [2], [3] require power-of-two FFTs. LTE uplink precoding requires nonpower-of-two discrete Fourier transforms (DFTs) from 12 to 2400. In the upcoming 5G [4] (the fifth generation mobile communication), FFT is still an essential algorithm for all of the waveform candidates, and the FFT computation speed should be high enough to support the highdata rate of 5G. Therefore, in the future multimode base station, the FFT processor should support diverse DFTs and high-speed FFTs. Many high-speed FFT processors [5]–[13] have been proposed for power-of-two FFTs. However, there are a limited number of processors supporting nonpower-of-two DFTs. Processor in [14] adds an extra radix-3 unit to support the 1536-point DFT in 4G LTE. The single-path delay feedback (SDF) architecture in [15] supports 48 2m3n points using 6T-RC processing element and section-based twiddle factor (TF) generator (STFG). SDF processor in [16] supports 46 2m3n5k points using a single-table approximation method (STAM) for TF generation. However, the throughput is restricted to 1× clock rate because of the limitation of the single-path pipelined architecture. Processors in [17] and [18] support 128- to 2048-point FFTs and 12- to 1296-point DFTs and use the prime factor algorithm (PFA) to minimize the number of TF multiplication. However, the data access of PFA cannot be in parallel for data I/O (read in input and write out result). The throughput is thus restricted to 1× clock rate and cannot meet the high-speed requirement for future 5G. There are still challenges in designing a low-power high-speed yet flexible processor for DFTs and FFTs. To design a high-speed processor supporting DFTs and FFTs, several aspects should be considered, including: 1) butterfly unit(s) supporting 2-, 3-, 5-, and higher radices; 2) TF multiplication scheme with hardware efficiency, and 3) conflict-free data access scheme that supports multiple butterfly units for 2-, 3-, 5-, and higher radices as well as minimizes the memory usage for nonpower-oftwo DFTs. In this paper, the contributions are to propose a memory-based FFT

ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024

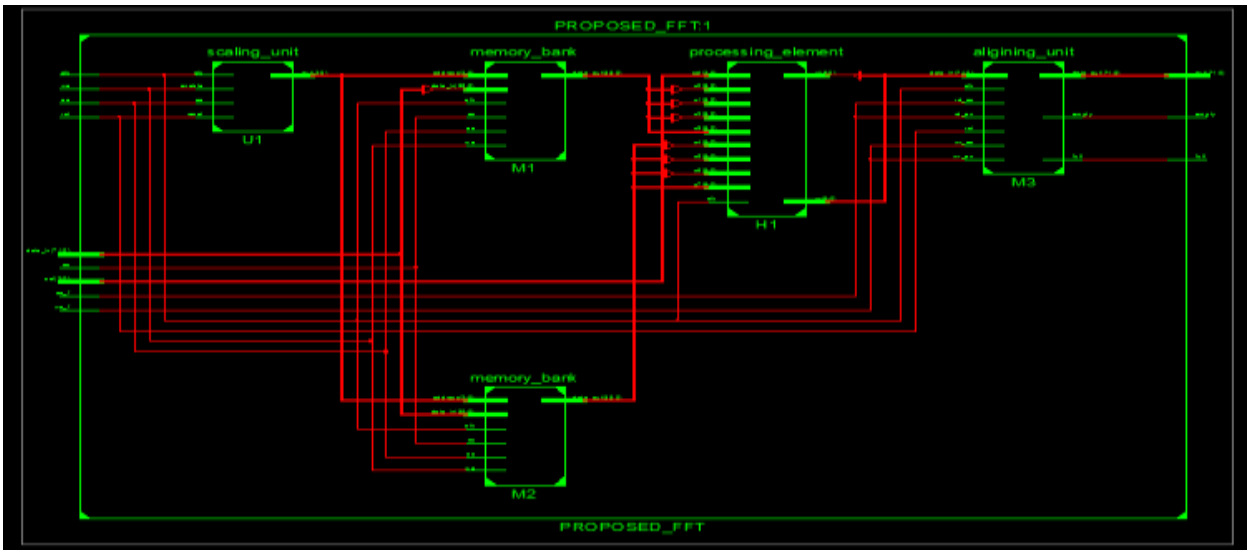
processor supporting 54 modes including 16-4096 point FFTs and 12-2400 point DFTs for 4G, WLAN, and future 5G and propose improvements on critical parts in butterfly unit, TF multiplier, and data access scheme. By reusing the hardware resources under timing constraint,

## RESULTS AND DISCUSSIONS:

RTL SCHEMATIC:




INTERNAL RTL SCHEMATIC:



INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024

DESIGN SUMMARY:

AREA

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Total Number Slice Registers | 412 | 17,344 | 2% | |
| Number used as Flip Flops | 124 | | | |
| Number used as Latches | 288 | | | |
| Number of 4 input LUTs | 664 | 17,344 | 3% | |
| Number of occupied Slices | 504 | 8,672 | 5% | |
| Number of Slices containing only related logic | 504 | 504 | 100% | |
| Number of Slices containing unrelated logic | 0 | 504 | 0% | |
| Total Number of 4 input LUTs | 670 | 17,344 | 3% | |
| Number used as logic | 592 | | | |
| Number used as a route-thru | 6 | | | |
| Number used as 16x1 RAMs | 72 | | | |
| Number of bonded IOBs | 156 | 304 | 51% | |
| Number of BUFGMUXs | 2 | 24 | 8% | |
| Number of MULT18X18SIOs | 8 | 28 | 28% | |
| Average Fanout of Non-Clock Nets | 2.61 | | | |

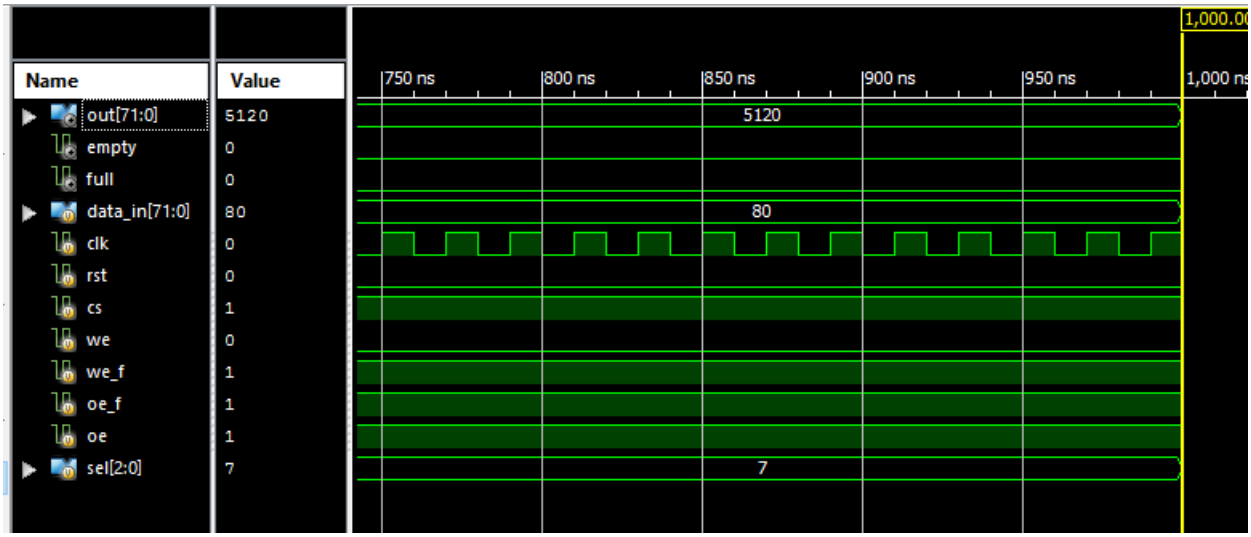
DELAY

```
    ----------------------------------------
    Total                          5.651ns (4.573ns logic, 1.078ns route)
                                           (80.9% logic, 19.1% route)

=========================================================================


Total REAL time to Xst completion: 35.00 secs
Total CPU time to Xst completion: 34.77 secs
```

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940
www.ijsem.org
Vol 15, Issuse . 1 Feb 2024

SIMULATION RESULTS




CONCLUSION

In this brief, for the first time a systematic design method for reconfigurable CORDIC is proposed to let a CORDIC function in different modes and different trajectories of operations. The proposed reconfigurable CORDIC architectures can be used in a variety of applications, such as synchronizers, waveform generators, low-cost scientific calculators, and so on. Approximately 60% of the area is saved by the proposed rotation or vectoring-mode reconfigurable CORDIC designs over the reference recursive reconfigurable CORDIC, without any effect on the maximum operating frequency. On the other hand, the proposed pipelined rotation and vectoring-mode reconfigurable CORDIC designs save 30%–50% area compared with the reference reconfigurable design, with nearly the same maximum operating frequency

REFERENCES

[1] C.-L. Yu, K. Irick, C. Chakrabarti, and V. Narayanan, “Multidimensional DFT IP generator for FPGA platforms,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 4, pp. 755–764, Apr. 2011.
[2] C.-H. Yang, T.-H. Yu, and D. Markovic, “Power and area minimization of reconfigurable FFT processors: A 3GPP-LTE example,” IEEE J. Solid-State Circuits, vol. 47, no. 3, pp. 757–768, Mar. 2012.
[3] D. Cohen, “Simplified control of FFT hardware,” IEEE Trans. Acoust., Speech, Signal Process., vol. 24, no. 6, pp. 577–579, Dec. 1976.

[4] M. C. Pease, “Organization of large scale Fourier processors,” J. ACM, vol. 16, no. 3, pp. 474–482, Jul. 1969.
[5] L. G. Johnson, “Conflict free memory addressing for dedicated FFT hardware,” IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 39, no. 5, pp. 312–316, May 1992.
[6] B. G. Jo and M. H. Sunwoo, “New continuous-flow mixedradix (CFMR) FFT processor using novel in-place strategy,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 5, pp. 911–919, May 2005.
[7] J. Baek and K. Choi, “New address generation scheme for memorybased FFT processor using multiple radix-2 butterflies,” in Proc. Int. SoC Design Conf., vol. 1. Nov. 2008, pp. I-273–I-276.
[8] D. Reisis and N. Vlassopoulos, “Conflict-free parallel memory accessing techniques for FFT architectures,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 11, pp. 3438–3447, Dec. 2008.