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Design and verification of low power high speed 9T Based SRAM at 16nm CMOS Technology.

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ABSTRACT
The main design characteristics for a static random-access memory (SRAM) cell are improved variation resistance, reduced power consumption, and dependability. Raising the voltage is the most direct route to reducing electricity use. The robustness of SRAM cells and the integrity of data are both compromised by the scaling of voltage at the nanoscale technological nodes. It is shown that traditional 6T SRAM has a decrease in stability as technology advances, particularly in the deep subthreshold area. Hold power is also somewhat power hungry, and SRAM cells with read decoupling for reliable read operation are considerably more power hungry. The great majority of today's Internet of Things devices operate in this way. Although the read and write access times are somewhat higher with a 9T SRAM that uses transmission gates, the method is more resilient and uses less hold power. A complementary metal oxide semiconductor with a size of 16 nm forms the basis of the models used in the simulations.

KEY WORDS: SRAM,10TSRAM,9TSRAM,LOWPOWER,

I.INTRODUCTION

Enhanced variation resistance, decreased power consumption, and reliability are the primary design attributes of a static random-access memory (SRAM) cell. Increasing the voltage is the quickest way to cut down on power use. However, data stability is compromised due to the SRAM cell's weakness caused by voltage scaling at nanoscale technological nodes. As technology progresses, the stability of typical 6T SRAM decreases, especially in the deep subthreshold region. In modern Internet of Things devices, SRAM cells—which rely on read decoupling and other methods to guarantee dependable read operation—consume an excessive amount of power. The result is a rise in both hold power and leakage current. A 9T SRAM that employs transmission gates has slightly longer read and write access times, but it is more durable and consumes less hold power overall. The calculations are based on a 16-nanometer-scale model of a semiconductor based on complementary metal oxides.

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II.LITERATURE SURVEY

Design and specification needs for various applications might vary greatly due to the dynamic nature of the electronics industry. As an example, although power consumption is a trade-off for performance in high-end applications like servers, GPUs, and general purpose computers, resilience and energy efficiency are the two most significant design requirements for BSNs and the IoT. Energy consumption is a major issue in all Internet of Things applications, regardless of how modest the average operating frequency range for these devices is—a few megahertz to a few megahertz. In Ultralow Power (ULP) Systems-on-Chip (SoCs), Static Random Access Memory (SRAM) is one of the primary sources of power loss in digital systems. The requirement for greater embedded memory, Consequently, a sub-threshold VDD is accessible, enabling the most effective decrease in energy usage throughout the design. Finding the optimal voltage that reduces the system's energy usage for each application requires exploring the design space and adjusting multiple knobs. For various performance goals and designs, this sweet spot will seem different. The threshold voltage of the transistors is a critical design parameter for building a reliable and power-efficient memory for IoT applications. We consider this when we investigate the SRAM design space.

III. EXISTING SE10 SRAM CELL

Figure 1 shows the design and the present condition of the control signals for the SE10T SRAM cell. Inverters M1–M7 provides a cross-coupled structure, while nodes Q and QB oversee data management. Word lines that control read-access transistors (RWL) and write-access transistors (WWL) are used in this circuit. While the WBL writes bits to the cell, the RBL reads bits from it. M10, a read-assist transistor, is passed via QB. Whenever the value of '0' is held or written, this transistor partly discharges the '0' that is stored at node Q.

As for the power-gating transistors M5 and M6, WWLB and WWLA are two possible controls. The suggested SRAM cell uses two bit lines (RWL and WWL) and two primary control signals (RBL and WBL); hence it only needs one more control signal than the standard 6T SRAM cell. This is because, as the picture indicates, the control signals WWL and Data_In are used to create two additional signals, WWLA and WWLB. Compose the Approach '1' through 'Q'. When WWLA and WWLB are pulled up, the power VDD rail is disconnected from QB, and WBL is set to GND by a write driver. The data is sent from WBL to QB and then discharged to GND after WWL is confirmed. After M3 is turned on, Q is charged to VDD. At this moment, M4 is activated and QB is discharged to ground via M5-M4. In Figure 4(b), you can see the numerals '0' through 'Q'. Connecting WBL to VDD with a write driver disables the power GND rail on QB. It follows that WWLA and WWLB are depressed. After that, M1 and M10 are activated when QB is charged via WBL-M9. Last but not least, Q is sent to ground via the M2-M1 and M10 pathways. A Vth-drop brought about by the p-type transistor M2 is corrected by the M10.

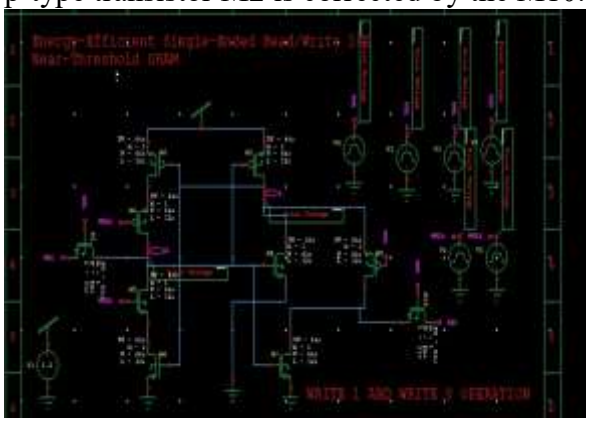

Fig: 3.1 TSRAM EXISITNG METHOD SCHEMATIC

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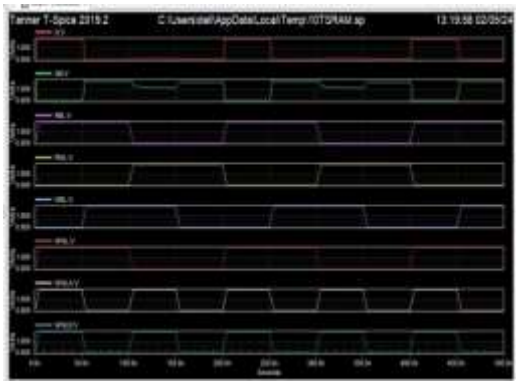


Fig: 3.2 simulation results OF EXISITNG METHOD

IV.PROPOSED SE9T SRAM CELL DESIGN

The suggested TG9T is shown in Figure 1. The various control signals used by various processes are listed in Table 1. When reading data from storage nodes Q and QB, at least one bit line is discharged. The cell may now write all the data it wants without worrying about the feedback channel (see Fig. 3). The bit line bar and bit line must be off at all times when the device is in hold mode, and access transistors must not be utilized.

Proposed schematic of 9T SRAM

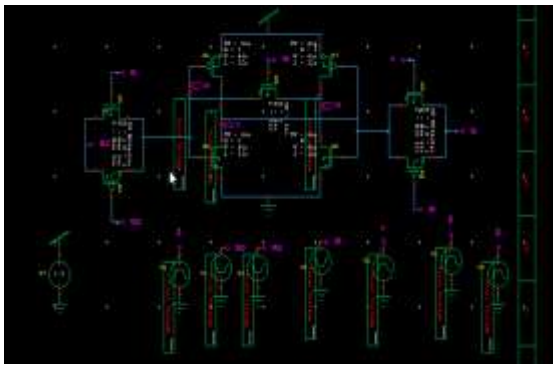


Fig: 4.1 SRAM EXISITNG METHOD SCHEMATIC

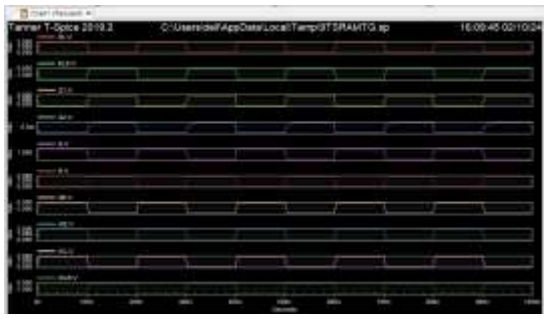
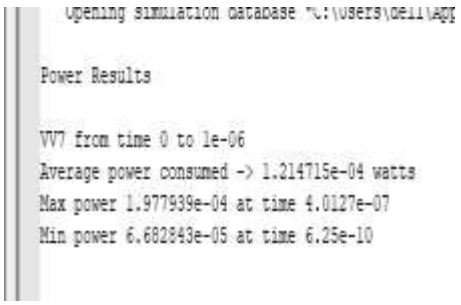


Fig: 4.2 SRAM EXISITNG METHOD SCHEMATIC

POWER ANALYSIS



COMAPRISON TABEL

S.NO	METHOD	TECHNOLOGY	AVG POWER	STATIC POWER	DYNAMIC POWER
1	10TSRAM	32nm	590mwatts	800mwatts	400mwatts
2	9T SRAM	16nm	1.25e-04	1.939e-04	6.643e-05

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Improved the write capabilities of a 6T SRAM cell by adding an additional transistor to allow loop-cutting during writes. Regrettably, the read stability has not been much improved by this cell. In an attempt to enhance read stability, read decoupling circuitry has been used. There are a number of proposed SRAM cells in that employ this technique. Using separate read ports allows them to complete read operations uninterrupted. Some disadvantages include the fact that they demand more space in the cell, leakage along data-dependent bit lines, and issues with detecting the margins while reading or providing extra paths for leakage currents to travel.

A. The Art of Reading

there is less variation in read operations when TGs are used in the proposed cell. Because they average their effects, this is caused by the two transistors in the TG that are connected in parallel. The characteristics of TG itself may provide a straightforward explanation for this (see to Figures 4-6). Figure 6 is the most effective representation of the TG effective resistance, which may be expressed as RE=RN||RP. While a rise in Vout (VQB) generates an increase in current flowing through a P-type metal oxide semiconductor (PMOS), a fall in RN causes a drop in current flowing through an N-type metal oxide semiconductor (NMOS). Figure 6 shows that the effective resistance of TG is almost constant throughout a broad voltage range, which means that the current flowing through this parallel combination of NMOS and PMOS stays constant. The net current through the TG may be stabilized and averaged using this approach. That IREAD via TG is more stable than IREAD via NMOS seems like the most sensible conclusion to draw.

B.WRITE Operation

Miniaturization of devices is largely responsible for the advancements in semiconductor integrated circuit technology. The supply voltage has remained mostly unchanged despite the device's shrinkage. Stronger electric fields over the gate oxide and in the pinch-off area have been seen as a result of the rise in MOSFET scaling. In a as an electron moves from the source to the drain of a metal-oxide field-effect transistor (MOSFET), its state changes. Permeability of the SiO2 barrier to a small fraction of the hot electrons is necessary for the production of the gate leakage current (IG). When more heated electrons contact with Si atoms en route to the drain, impact ionization creates secondary electron-hole pairs. It is possible to generate soluble current (IB) by collecting electrons using the positive drain bias and holes using the negative body bias.

A 9T SRAM cell using the proposed method represents a significant advance in memory technology. Using novel circuit design approaches and an increase in transistor density, this approach aims to overcome the limitations of conventional 6T SRAM cells. A critical component, the system's stability is enhanced by adding more read and write paths, making it less susceptible to noise and disturbances. In order to minimize power consumption, the proposed 9T SRAM cell makes use of aggressive voltage scaling and leakage current minimization approaches. In keeping with the growing need for energy-efficient electronics, this contributes to better power management. Error correction codes and built-in self-repair systems are reliability components that further increase data integrity and fault tolerance. On the whole, the proposed practical method for a 9T SRAM cell provides a promising direction for addressing the growing memory system requirements of contemporary computer applications.

VI.CONCLUSION

For IoT applications, we provide a TG9T SRAM cell. The majority of the studies have included TG9T comparisons to other small

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SRAM cells including FD8T, 7T, and SEDF9T (single-ended read-disturb-free 9T). Because of the decreased leakage currents, the hold power of the proposed cell is 1.25×/1.53× less than 7T/SEDF9T. When compared to 7T/FD8T, it consumes 1.17 times less power during read operations and 1.07 times less power during write operations. With WSNM that is 1.42×/5.3× higher and RSNM that is 1.40×/1.80× higher, the TG9T surpasses the FD8T/SEDF9T and 7T/FD8T in regard to write ability and read stability. Furthermore, the proposed cell exhibits less variation in all experimental variables. Furthermore, TG9T outperforms 7T/FD8T/SEDF9T by a margin of 1.22×/1.60×/1.88×, operating at the lowest VDD, min. Even though the RSNM is lower than SEDF9T and the read/write latency is somewhat higher than 7T and FD8T, the benefits outweigh the drawbacks. According to Table 6, the cell with the highest EQM/V2EQM is TG9T. We believe our proposed TG9T SRAM cell is perfect for IoT applications because to its low power consumption, durability, and reliability.

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