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E-Mail :
editor.ijasem@gmail.com
editor@ijasem.org

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LOW POWER HIGH SPEED AND EFFECTIVE AREA DESIGN OF GDI HYBRID ONE BIT FULL ADDER USING CMOS TECHNOLOGY.

SHAISTHA M.Tech P.G Scholar[1], Dr. Y.David Solomon Raju Associate .Professor[2]

ABSTRACT

We are working on the project. Using the Mentor Tanner tool and 16 nm CMOS technology, we set out to create a novel FA architecture that maximizes efficiency while reducing power expenditure. In this simulation, the design's performance is assessed using PDP, propagation delay, and power dissipation as measures. Our proposed FA design has the smallest propagation, according to the simulation findings. latency and highest power consumption. Dissipation across all investigated frequency and voltage ranges. The suggested GDI hybrid one-bit full adder has a 10T design and consumes less power; it has a latency of 739.2364p, an average power consumption of 2.663027e-07 watts, a maximum power consumption of 3.204438e-06, and a minimum power consumption of 3.587541e-10. As a result, the proposed adder's efficiency increases as the number of computations increases.

I. Introduction

Virtually every kind of digital CMOS VLSI system, from microprocessors to GPUs, relies on adders, one of the most ubiquitous mathematical functions. Full Adders (FAs) and other multi-bit operations like addition, multiplication, and subtracting rely on them. Because of its position on the system's critical route, the FA's performance frequently impacts the entire performance of the system. Portable, high-powered, and energy-efficient gadgets are in high demand in the present day. This is why there has been a recent uptick in interest in low-power circuit blocks among electronics manufacturers. The reason for this is because they will provide the groundwork for the creation of battery-powered gadgets that can last for extended periods of time. 3. This benefit, which enables devices to operate at higher frequencies, is essential for most computation-intensive applications today, since they need very fast throughput. Using a multi-bit adder circuit, the most fundamental mathematical operation of adding is carried out. Typically located in the microprocessor's Arithmetic and Logic Unit (ALU), multi-bit adders are essential to almost all digital VLSI systems.

[1,2]Holy Mary Institute of Technology & Science, Keesara - Bogaram - Ghatkesar Rd, Kondapur, Telangana 501301

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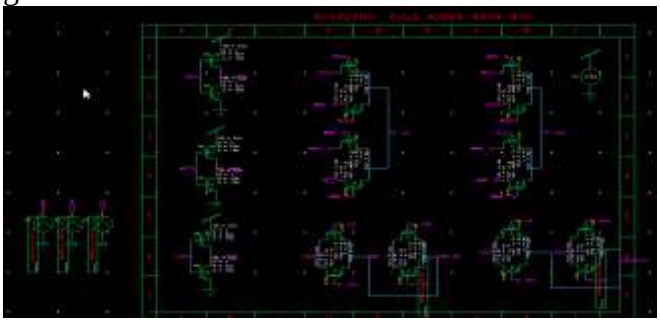
II.LITERATURE SURVEY

The functioning of a 1-bit full-adder cell is examined in this study. Some of the adder cell's components have been extracted. I spent a considerable amount of time investigating and testing the modules. For each of them, we build, test, and evaluate a number of design iterations. Twenty distinct by mixing several designs of these modules, 1-bit full-adder cells are constructed; most of these cells are new circuits. There are a variety of these cells, and some are more powerful, smaller, and quicker than others. The inclusion of adder cells is limited to one of the two real-world circuit designs included in the simulation. To aid circuit designers in their search for the perfect full-adder cell, we have compiled this collection of cells. There are few mathematical operations as foundational as the addition operation. It finds widespread usage in VLSI systems, particularly in microprocessors and designs for application-specific digital signal processing (DSP). The most common usage is to add two binary integers, but it is also the foundation for many other important operations including subtracting, multiplying, dividing, and calculating addresses, among many others. The adder plays an essential role in the critical path of the majority of these systems, which dictates the system's performance. Because it forms the basis of the binary adder, the 1-bit full-adder cell must be optimized for maximum efficiency. As mobile computing and communication continue to advance at a rapid pace, there is a growing demand to construct VLSI systems with low power consumption. When compared to microelectronics, battery technology is falling behind. The amounts of power that can be used by mobile systems are restricted. Another set of limitations that designers have to work with include things like speed, low power consumption, and limited silicon area. Consequently, developing efficient adder cells that do not deplete the battery is a highly debated subject.

III.EXISTING METHOD

Our two new Low Power Hybrid Full Adder (LPHFA) designs integrate CMOS FA with twenty-two different semiconductors and eighteen transistors. Both FA designs consist of an inverter, an XOR-XNOR, and a multiplexer (MUX). The Inverter (Step 3.1) The XOR-XNOR and MUX stages rely on the inverter stage to produce the altered input signals. In the LPHFA FA scheme, A, B, and Can are all made by matching semiconductors between MP1-MN1, MP2-MN2, and MP3-MN3, in that order. Although the XOR-XNOR stage utilizes the and B signals, the MUX stage forms Sum using Cin. Moreover, signals B and C, respectively, are generated using the LPHFA FA technique by use of the MP1-MN1 and MP2-MN2 semiconductor matches.

In order to regulate the decision line of a 2-input transmission doorway type multiplexer, the XOR and XNOR signals are created at this level of the MUX stage. The LPHFA and LPHFA FA designs used different approaches to build the XOR-XNOR stage. We reduced the LPHFA FA plan's expansion time by sending the XOR and XNOR signals at the same time. The MUX stage receives these signals as a guarantee line.



3.1 EXISITNG FULL ADDER WITH MUX

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The XOR and XNOR indications are sent by DPL, or Double Pass Semiconductor Logic [46]. Below are the Boolean criteria that are used to construct the XOR and XNOR signals in an LPHFA FA plan. Next, the output is multiplied by the equation that follows: The following equation describes LPHFA: MP4-MP5-MN4-MN5. In XNOR, the set of all potential bases is LPHFA: MP6-MP7-MN6-MN7, which is the same as AB plus AB. As part of the LPHFA plan, and

3.2 SIMUALTION OF EXISITNG FULL ADDER WITH MUX

Reducing the distribution of electricity became our primary focus. Possible XNOR signals for reducing power dispersion by reducing the number of semiconductors in the design

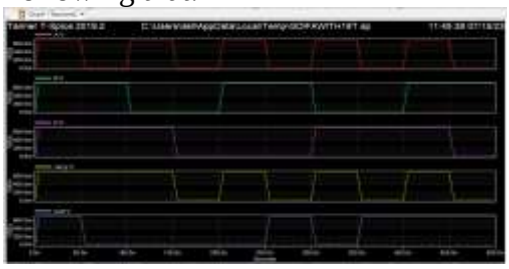
In comparison to the XOR-XNOR design employing the DPL style [3], sometimes called the invertible inverter and transmission entryway XNOR [4], which uses eight semiconductors, the LPHFA design uses six. Similarly, the configuration proposed in [3] does not need an A sign, resulting in one fewer inverter being required for the Inverter stage.

3.3 Schematic of Existing Full Adder with Mux-18t

It is possible to eliminate four semiconductors from the design as a whole, but doing so would require sacrificing the nonconcurrent age of the XOR and XNOR signs, which might cause the FA's generation latency to rise. The following Boolean criteria are used by the LPH to create XOR and XNOR signals. Approach to FA

XOR = XNOR (LPHFA: MP5-MN5)
XNOR = AB + AB (LPHFA: MP3-MP4-MN3-MN4)
MUX Stage

Sum and Cout yields are often generated by transmission entry type multiplexers in several FA systems [1, 3, 23, 25, 33, and 47]. Reproduction results in [30] show that FAs outfitted with transmission entry type multiplexers often have lower PDP values. Following that.



3.4 Simulation of Existing Full Adder with Mux-18t

In all of our FA systems, Cout and Sum are generated using a transmission entry type multiplexer. The multiplexers make their decisions based on the XOR and XNOR signals that are produced by the XOR-XNOR stage. In contrast to the multiplexer that produces Cout, which produces an, the multiplexer that produces Sum provides Cin and Cin. Finally, the sum and cost yields expressed in Boolean notation are

Sum = Cin(A`B) + Cin(AbB) (LPHFA: MP8-MP9-MN8-MN9)
(LPHFA: MP6-MP7-MN6-MN7)
(LPHFA: MP8-MP9-MN8-MN9)

IV PROPOSED METHOD

Proposed GDI one bit Full adder

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The one-bit complete adder that is proposed employs 10 transistors and the GDI method to build it. A total of ten transistors—five PMOS and five NMOS—are required. The GDI techniques are used by all of the complete adder designs that have been discussed. All it takes to make an adder work is 10 transistors.

As part of its design, this circuit Figure shows that just fourteen semiconductors are needed for the whole snake design. The five logic blocks that make up the circuit were all created using the MVT-GDI approach. These blocks include two multiplexers, an XOR/XNOR block, an SRPT block, and an SRTG, or Swing Restored Transmission Gate.

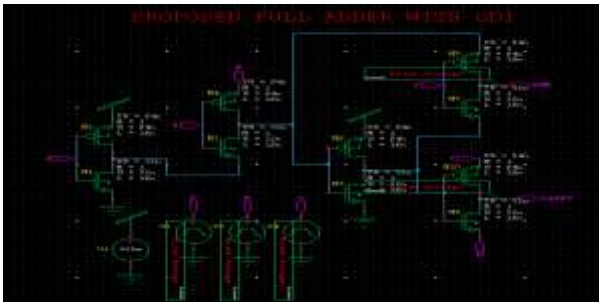

Fig 4.1 Schematic of proposed one bit GDI Full adder using SEDIT

The following schematic depicts a 16 nm hybrid full adder that makes use of 10T transistors, with 5 PMOS and 5 NMOS logic gates. The Tanner S-EDIT Tool was used in its creation.

You can see the Hybrid Full GDI Adder-10T Transistor's simulation results up there. The CMOS Tanner-SPICE simulation program, which focuses on integrated circuits, is used for this purpose. If you want to analyze wave forms, you should use the wave form editor, or W-EDIT.

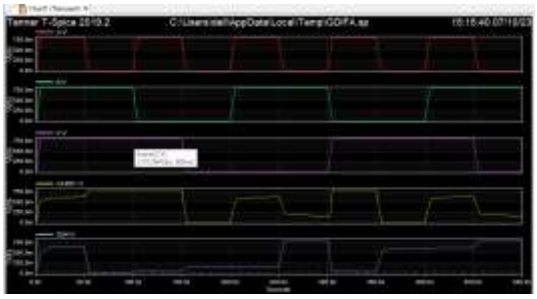

Fig 4.2 Simulation of proposed one bit GDI Full adder using SEDIT

The previous simulation picture shows A=100 nm, B= 200 nm, and C= 300 nm. Where A, B, and C are all zero, the total and carry are also zero. If numbers A, B, and C are all zero, then the total is one and the carry is zero. The sum and carry will both be 0 if A, B, and C are all zeros. A total of '0' and a carry of '1' will result from A0= 0, B= 1, and C = 1. In the case when A=1, B=0, and C=0, the sum equals "1" and the carry is false. If A=1, B=0, and C=1, then the total will be '0' and the carry will be '1'. When A=1, B=1, and C=0, the sum is '0,' and the carry is '1' accordingly. The sum and carry are both 1 if A= 1, B= 1, and C= 1.

Syntax

.power VV1

.measure trantdealy trig v (A) Val=0.5 fall=0.5 targ v (SUM) Val=0.5 fall=0.5

Power analysis

```
Power Results

VV1 from time 0 to 8e-07
Average power consumed -> 1.0384164e-06 watts
Max power 9.189482e-06 at time 3.020594e-07
Min power 1.766397e-09 at time 2.5875e-07


Measure information will be written to file 'C:\Users\dell\AppData'

Measurement result summary
   tdealy          = 739.2364p
```

Comparison table

S.No	Methodology	Avag Power	Max Power	Min Power	Area	Delay
1	XOR-XNOR	5.035416e-06	8.189482e-06	8.5841e-6	28	96.56n
2	XOR-XNOR	3.035416e-06	6.189482e-06	5.5841e-6	22	78.2364n
3	GDI	3.035416e-06	5.189482e-06	6.5841e-6	24	94.2364n
4	MUX	2.035416e-06	4.189482e-06	4.5841e-9	18	68.2364n
5	GDI	1.035416e-06	9.189482e-06	5.5841e-10	10	739.2364p

V.CONCLUSION

The goal of this study is to create three hybrid adders that work perfectly. Using full swing XOR, OR, and AND gate logic, this

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design boosts driving capabilities for cascaded operation and reduces the GDI threshold voltage problem. Faster operation and lower voltage result in reduced power consumption, which is a direct result of better driving capabilities. This experiment made use of the Mentor Tanner 16 nm Device.A power analysis is not performed until all of the designs mentioned above have been fully simulated. The proposed 10T GDI hybrid one-bit full adder uses less power, has a latency of 739.2364p, and has an average power usage of 2.663027e-07 watts with a high of 3.204438e-06 and a minimum of 3.587541e-10. However, it does have lower power consumption. Consequently, the efficiency of the suggested adder improves with increasing numbers of calculations.

Decade End Objectives In comparison to the conventional complementary metal-oxide semiconductor (CMOS) approach, the energy consumption of gate-drive integrated circuits (GDIs) is lower. A lower footprint, less propagation delay, and fewer transistors are further benefits of GDI. Consequently, the efficiency of the suggested adder improves with increasing numbers of calculations. Many types of microprocessors and digital signal processors are included in this category.

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