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DESIGN AND EXECUTION OF CARRY INCREMANT ADDER USING HAN-CARLSON AND KOGGESTONE

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ABSTRACT

This project sets out to harness the power of these advanced techniques by integrating them into the design of a Carry Increment Adder (CIA). The CIA architecture, renowned for its parallel processing capabilities and reduced carry propagation delay, serves as an ideal platform for the implementation of these enhancements.

Through meticulous design and execution, this project endeavours to achieve significant improvements in the speed, efficiency, and overall performance of binary addition operations. By synergistically leveraging the strengths of the Han-Carlson and Kogge-Stone adder techniques within the CIA framework, the aim is to create an Enhanced Carry Increment Adder that sets new benchmarks in the realm of high-speed arithmetic computations.

With a focus on innovation and optimization, this project not only seeks to advance the state-of-the-art in adder design but also aims to contribute to the broader landscape of digital circuitry and computational efficiency. Through rigorous experimentation and analysis, it endeavors to demonstrate the tangible benefits of its proposed enhancements, paving the way for future advancements in computer arithmetic and digital system design.

INTRODUCTION

In the realm of digital circuit design and computer arithmetic, the pursuit of faster and more efficient adder architectures is perpetual. The project "Design and Execution of Enhanced Carry Increment Adder using Han-Carlson and Kogge-Stone adder Technique" embarks on this journey, aiming to push the boundaries of performance and optimization in binary addition operations.

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Traditional adder circuits, such as the ripple carry adder (RCA), while conceptually simple, suffer from inherent limitations in terms of speed due to their serial nature of carry propagation. To address this challenge, innovative techniques like the Han-Carlson and Kogge-Stone adder methodologies have emerged, offering promising avenues for enhancing adder performance.

This project sets out to harness the power of these advanced techniques by integrating them into the design of a Carry Increment Adder (CIA). The CIA architecture, renowned for its parallel processing capabilities and reduced carry propagation delay, serves as an ideal platform for the implementation of these enhancements.

Through meticulous design and execution, this project endeavours to achieve significant improvements in the speed, efficiency, and overall performance of binary addition operations. By synergistically leveraging the strengths of the Han-Carlson and Kogge-Stone adder techniques within the CIA framework, the aim is to create an Enhanced Carry Increment Adder that sets new benchmarks in the realm of high-speed arithmetic computations.

LITERATURE SURVEY

1.Paper Title: "A Fast Parallel Hybrid Adder for Embedded Microprocessor Systems" (2015):

Disadvantages: Although the Han-Carlson adder offers improved performance over traditional adders, it may still suffer from high power consumption and area overhead, particularly when implemented in complex systems with large word sizes.

2. Paper Title: "A Parallel Prefix Adder Implemented with a Reconfigurable Logic Cell Array" (1981) Authors: Peter Kogge, Harlan E. Stone

Disadvantages: The Kogge-Stone adder technique can exhibit high area overhead due to its extensive use of logic resources. Additionally, it may require complex routing and wiring, which can lead to increased delay and power consumption.

3. Paper Title: "Design and Analysis of High-Performance Carry-Increment Adder" (2019)

Authors: Alok Rathi, Anu Gupta

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Disadvantages: This paper presents a traditional carry-increment adder design but may lack the advancements proposed in newer techniques like Han-Carlson and Kogge-Stone, potentially leading to inferior performance in terms of speed and efficiency.

4. **Paper Title: "Performance Analysis of Carry Select Adder, Carry Increment Adder and Carry Lookahead Adder in 90nm Technology" (2017)**

Authors: S. Santhi, M. Kavitha, M. Shalini

Disadvantages: While this paper compares different adder designs, including carry increment adders, it might not specifically address the enhanced versions incorporating Han-Carlson and Kogge-Stone techniques. Thus, it may not provide insights into the latest advancements in this area.

PROPOSED METHODOLOGY

The proposed system "Design and Execution of Enhanced Carry Increment Adder using Han-Carlson and Kogge-Stone Adder Techniques" aims to address these disadvantages by introducing enhanced designs based on the Han-Carlson and Kogge-Stone techniques. These techniques offer several advantages over conventional designs, including:

Reduced Propagation Delay: The Han-Carlson and Kogge-Stone techniques leverage parallel processing and optimized carry generation methods to minimize propagation delay, resulting in faster arithmetic operations and improved overall system performance.

Lower Area Overhead: By employing more efficient logic structures and optimized circuitry, the proposed system can achieve a reduced area footprint compared to conventional designs. This allows for better integration into modern semiconductor devices with limited physical space and power budgets.

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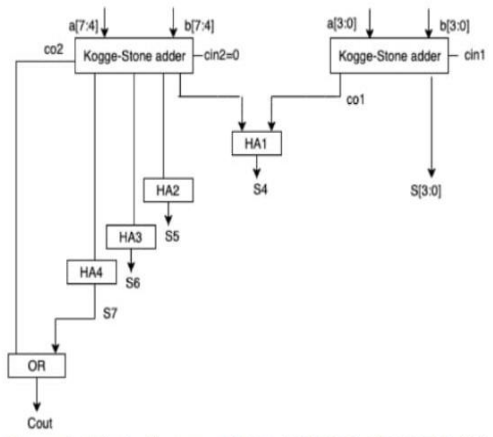

Figure 3. Block diagram of CIA_KOGGE-STONE(8-bit)

Figure.1 CIA_KOGGE_STONE

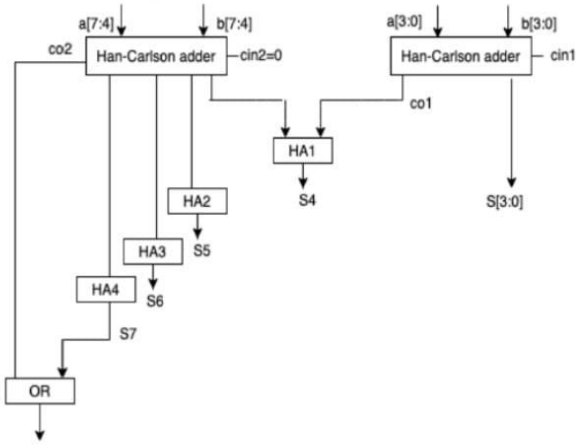

Figure 4. Block diagram of CIA_HAN-CARLSON(8-bit)

Figure.2 CIA_HAN_CARLSON

SIMULATION & SYNTHESIS RESULTS

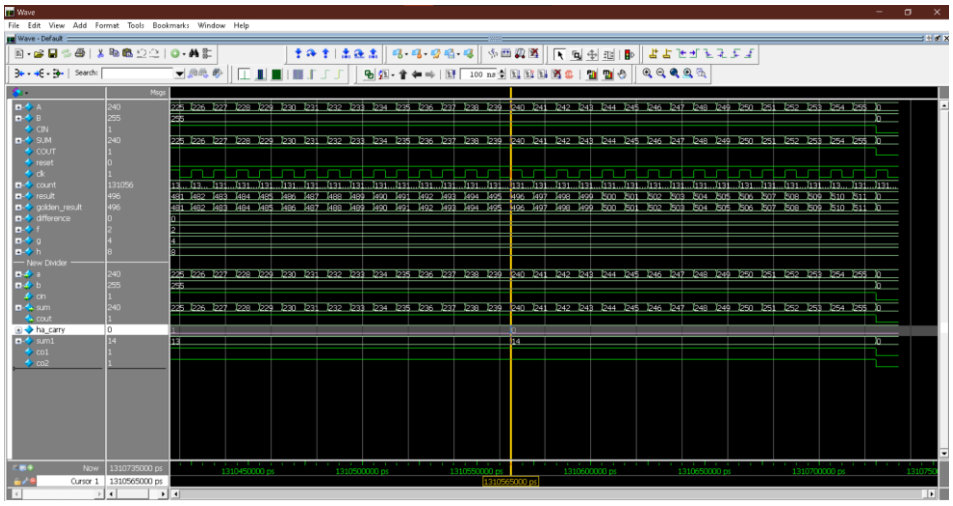

Figure.3 Simulation Results 16bit CIA-KSA

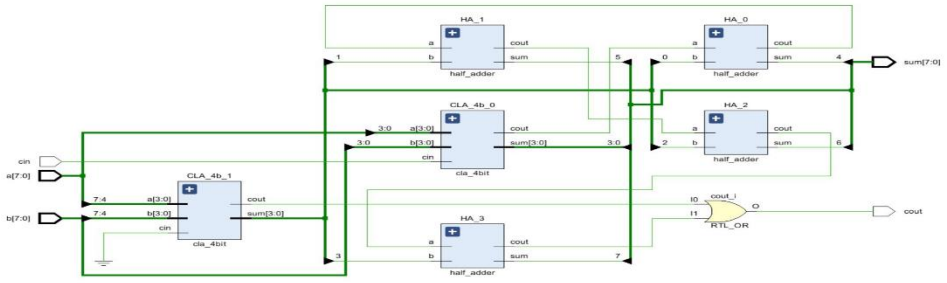

Figure.4 Schematic_CIA-CLA-8

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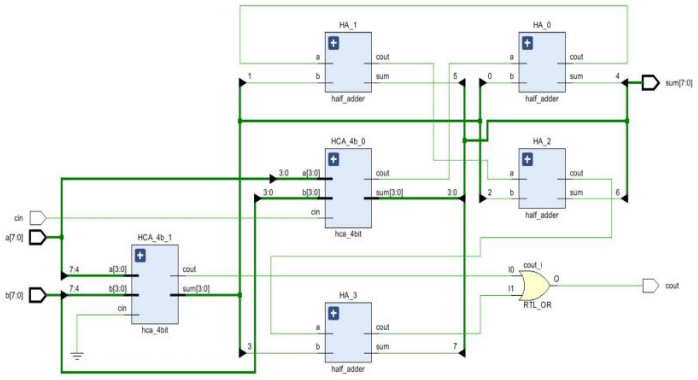

Figure.5 Schematic _CIA_HCA_8

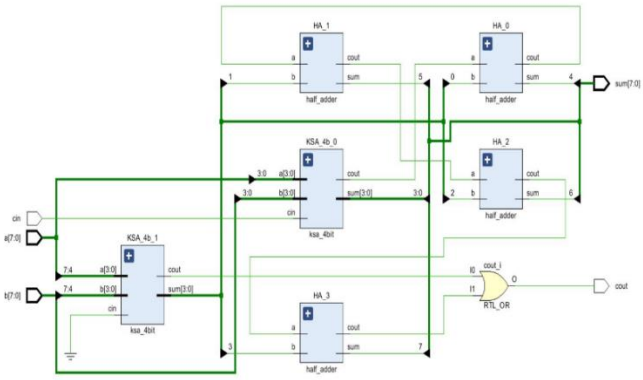

Figure.6 Schematic_CIA_KOGGESTONE_8

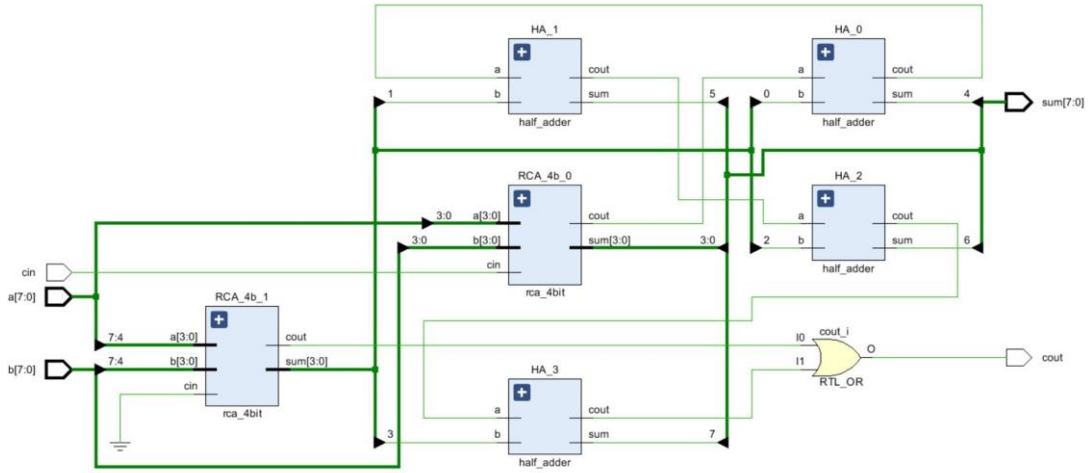

Figure.7 Schematic _CIA_RCA_8

Area Report CIA-CLA 8bit

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	11	0	303600	<0.01
LUT as Logic	11	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
IBUF	17	IO
OBUF	9	IO
LUT6	5	LUT
LUT5	5	LUT
LUT3	3	LUT
LUT4	2	LUT

Area Report CIA-HCA 8bit

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LUT as Logic	13	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
IBUF	17	IO
OBUF	9	IO
LUT6	6	LUT
LUT5	5	LUT
LUT3	4	LUT
LUT4	1	LUT
LUT2	1	LUT

Area Report CIA-KSA 8bit

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	13	0	303600	<0.01
LUT as Logic	13	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
IBUF	17	IO
OBUF	9	IO
LUT6	6	LUT
LUT5	5	LUT
LUT3	4	LUT
LUT4	1	LUT
LUT2	1	LUT

Area Report CIA-RCA 8bit

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	12	0	303600	<0.01
LUT as Logic	12	0	303600	<0.01
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
IBUF	17	IO
OBUF	9	IO
LUT6	6	LUT
LUT5	6	LUT
LUT3	3	LUT
LUT4	1	LUT
LUT2	1	LUT

ADVANTAGES

Improved Performance: By incorporating the Han-Carlson and Kogge-Stone adder techniques, the project aims to enhance the performance of carry increment adders (CIA). These techniques have been proven to reduce delay and improve speed compared to traditional adder designs, leading to more efficient arithmetic operations.

Reduced Circuit Complexity: The utilization of Han-Carlson and Kogge-Stone adder techniques results in a reduction in complex circuitry. This streamlined design not only simplifies implementation but also helps in reducing area overhead, making it suitable for constructing large adders efficiently.

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APPLICATIONS

Digital Signal Processing (DSP): In DSP applications such as audio and video processing, real-time signal filtering, and image recognition, high-speed arithmetic operations are essential. The enhanced carry increment adder can improve the performance of DSP algorithms by reducing processing time and enabling faster execution of complex mathematical operations.

Embedded Systems: Embedded systems used in automotive, aerospace, industrial automation, and IoT devices often require efficient arithmetic operations for real-time control and data processing. The enhanced carry increment adder can enhance the performance of these systems by enabling faster computation of sensor data, control algorithms, and communication protocols.

High-Performance Computing (HPC): In HPC applications like scientific simulations, weather forecasting, and computational fluid dynamics, the speed of arithmetic operations directly impacts overall system performance. By integrating the enhanced carry increment adder into processors and accelerators, HPC systems can achieve higher throughput and reduced execution time for computational tasks.

Real-Time Control Systems: In applications such as robotics, autonomous vehicles, and industrial control systems, real-time processing of sensor data and control signals is critical for ensuring safe and efficient operation. The enhanced carry increment adder can facilitate faster computation of control algorithms, enabling more responsive and accurate control of physical systems.

CONCLUSION

The conclusion drawn from the above work indicates that the CIA_HAN-CARLSON design offers a notable reduction in complex circuitry compared to the KOGGE-STONE adder. This reduction presents a significant advantage when constructing large adders. Therefore, the CIA_HAN-CARLSON design provides a favourable trade off, balancing complexity and efficiency.

In terms of performance, the CIA_HAN-CARLSON exhibits reduced delay for the same n-bit configuration compared to other adder designs such as CIA_RCA, CIA_CLA, and CIA_KOGGE-STONE. This reduced delay translates to faster operation, enhancing the overall

speed of complex circuitries where it is utilized. By employing CIA_HAN-CARLSON as the basic adder unit within complex circuitries, the overall speed of these circuits can be notably improved due to its lower delay compared to alternative adder circuitries. This improvement in speed can have significant implications for applications requiring high-speed arithmetic operations. Ultimately, the choice of which adder to use depends on the specific requirements of the application at hand. However, the findings suggest that CIA_HAN-CARLSON presents a compelling option for scenarios where reducing delay and enhancing speed are critical factors.

FUTURE SCOPE

Optimization for Specific Applications: One potential direction for future research involves tailoring the enhanced carry increment adder (CIA) design to meet the specific requirements of various applications. By analyzing the characteristics and demands of different computing tasks, researchers can fine-tune the parameters of the adder to optimize its performance for tasks such as data processing, signal processing, or cryptography.

Integration into High-Level Architectures: Another area of interest is the integration of the enhanced CIA design into higher-level architectural frameworks, such as microprocessors, digital signal processors (DSPs), or system-on-chip (SoC) platforms. By incorporating the enhanced adder into these complex systems, researchers can evaluate its impact on overall system performance, power efficiency, and area utilization.

Exploration of Alternative Implementation Techniques: Researchers can explore alternative implementation techniques for the enhanced CIA design, such as utilizing emerging technologies like approximate computing, reversible logic, or quantum computing. These alternative approaches may offer novel solutions to challenges related to speed, power consumption, and scalability.

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