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IMPLEMENTATION OF EFFICIENT AND LOW POWER TEST PATTERN GENERATORS

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ABSTRACT

We are aware that during testing when the device's normal functioning mode is off, the dissipation of power is approximately 200% more than that of normal functioning mode. In this project 32-bit test pattern generator has been proposed for testing the VLSI design. This 32-bit test pattern generator is implemented with efficient LFSR and with extra combinational circuitry which achieved Low power consumption. The switching activity between the tests vector are reduced, this results in low power consumption .

INTRODUCTION

An evolution of current microelectronics industry allows us to make complex digital systems on a single microchip. To design such a system is not an easy task anymore because the increasing density raises a whole set of different problems such as size, speed and power consumption of the chip. Nowadays, Complex VLSI testing problems such as BIST technique has been implemented and widely studied. In the BIST, the test vectors are generated by using LFSR (Linear feedback shift register) and applied to the device under test (DUT) which increases the area overhead therefore, reducing area which is a vital problem for the realization of Built-in-self test. As BIST technique requires high hardware overhead, this results in the memory required is more to store precomputed test pattern.

The test vectors are generated by the random sequence test pattern which also known as LFSR. The LFSR is the sequential logic circuits used to create pseudorandom binary sequences (PRBSs). An LFSR circuit consists of a set of M registers and feedback taps that establish the sequence of states that the LFSR transitions through. The feedback taps are described by a modulo-2 polynomial. A primitive polynomial generates a maximal length of m-sequence,

where the LFSR transitions through the 2m-1 state before repeat sequences, there is a single unused LFSR state.

The PRBS is the binary output of the LFSR. The random binary sequence is described as pseudorandom, as the sequence is continuous in nature and that results from the correlation properties of a random sequence. Whereas in testing mode the power consumption increases due to following reasons: high switching activity between the two consecutive test patterns, during test mode sequential activation of internal core, power utilized by extra circuitry during circuit under test and low relationship between the two-test vector.

LITERATURE SURVEY

1."Low-power test pattern generation using low-transition linear feedback shift register" by F. Wagner and H.-J. Wunderlich.

This paper proposed a low power test pattern generator using a low-transition LFSR to reduce switching activity during test. The authors demonstrated that their method achieved significant reductions in power consumption without affecting test quality.

2. "A Low-Power Test Pattern Generator Using Low-Transition LFSR for SoC Test" by C. Kim, H. Shin, and K. Choi.

This paper presents a low power test pattern generator that utilizes a low-transition LFSR. The authors showed that their method achieved significant reductions in power consumption and peak power compared to existing methods.

3. "Design of low power test pattern generator using low-transition linear feedback shift register" by M. N. K. Prasad and B. P. Mohanty.

This paper proposed a low power test pattern generator using a low-transition LFSR that generates test patterns with low power dissipation. The authors demonstrated that their method achieved significant reductions in power consumption compared to existing methods.

4. "Design and implementation of a low power test pattern generator using low-transition LFSR" by S. Lee, H. Lee, and J. Kim.

This paper presents a low power test pattern generator that uses a low-transition LFSR and achieves significant reductions in power consumption and peak power. The authors demonstrated the effectiveness of their method through simulations and experiments.

5. "A Novel Low-Power Test Pattern Generator Using Low-Transition LFSR" by Y. Song, J. Kim, and D. Lee.

This paper proposed a novel low power test pattern generator that utilizes a low-transition LFSR and achieves significant reductions in power consumption compared to existing methods. The authors demonstrated the effectiveness of their method through simulations and experiments.

PROPOSED METHODOLOGY

This project focuses on low-power LT-LFSR based test pattern generator that can be used for testing of both combinatorial and sequential circuits. The proposed architecture step-up the correlation between the two tests vectors which reduces the number of transitions i.e. switching activities between two test vectors. Minimizing the switching activity between test vectors will result in reducing the power consumption. The conventional LFSR architecture is to be customized in such a way that it routinely injects intermediate patterns between its unique pair of patterns. This can be done by using two schemes i.e. Bipartite and random injection, which is further discussed in this section and with a minimal number of switching activity between two test vectors.

We propose a Low Transition Test Pattern Generator that introduces two techniques for test vectors generation called Random Injection (RI) and Bipartite LFSR. In brief, the RI technique injects a new pattern between two successive test patterns by using a random-bit injection (R) whether it can be either ‘0’ or ‘1’, in the consequent bit of an intermediate pattern where there is transition occurs in the corresponding bit of pattern pairs.

SIMULATION & SYNTHESIS RESULTS

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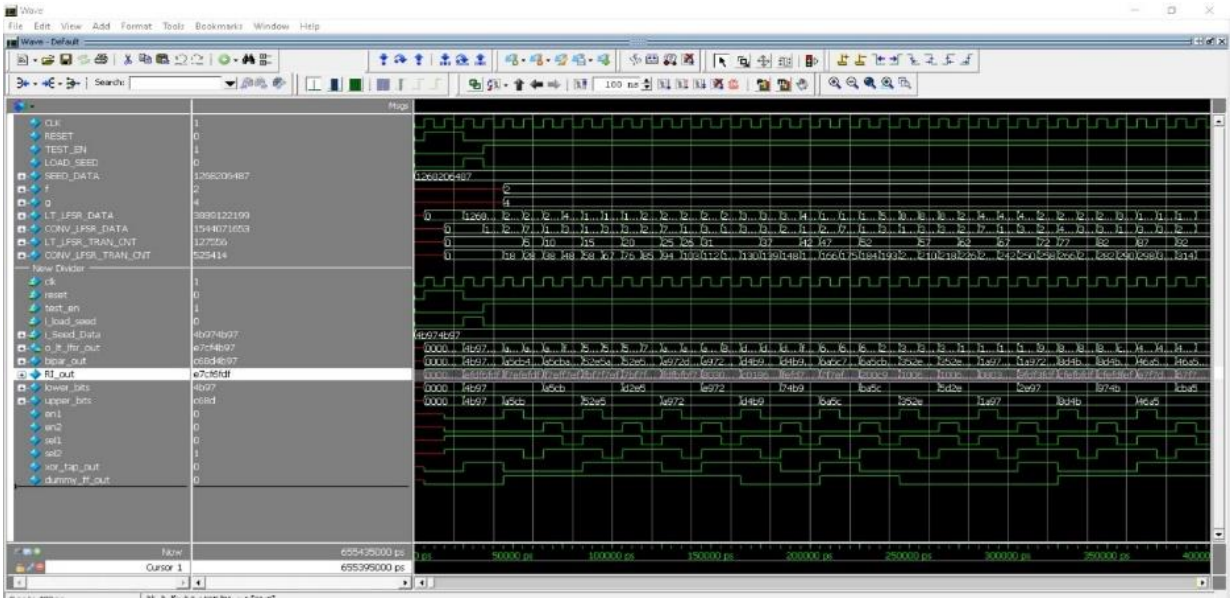

Figure.1 Stimulation result1

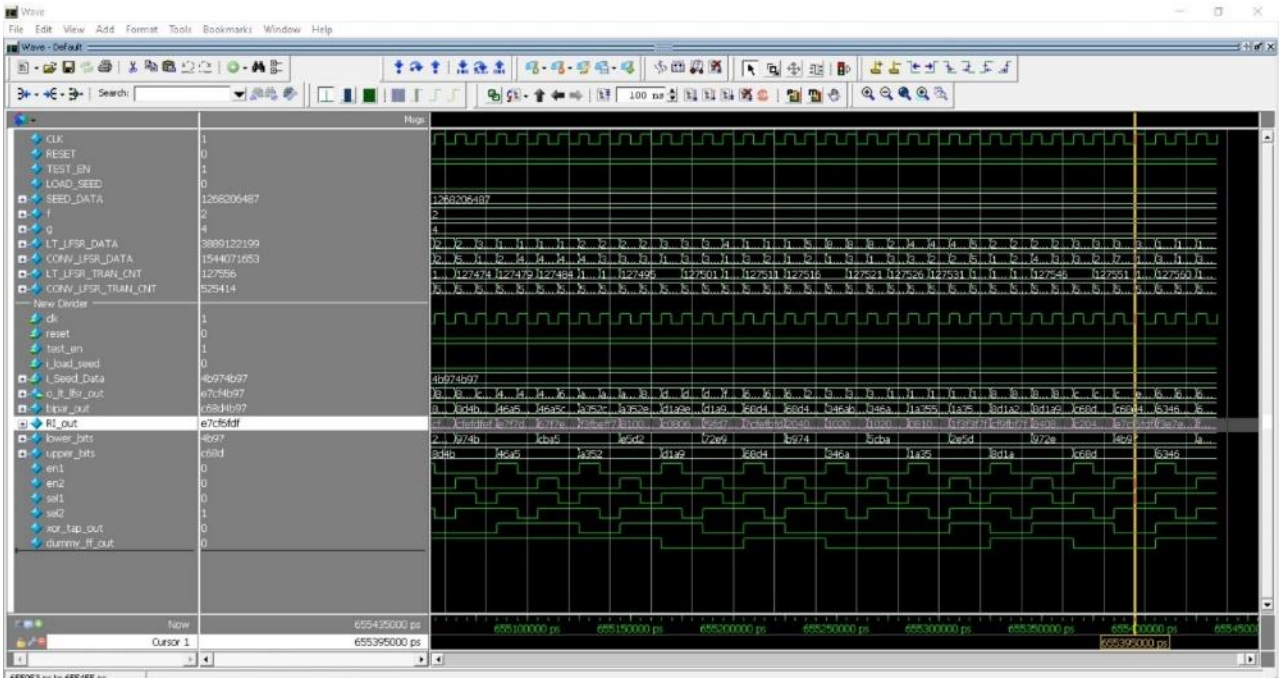

Figure.2 Simulation Result2

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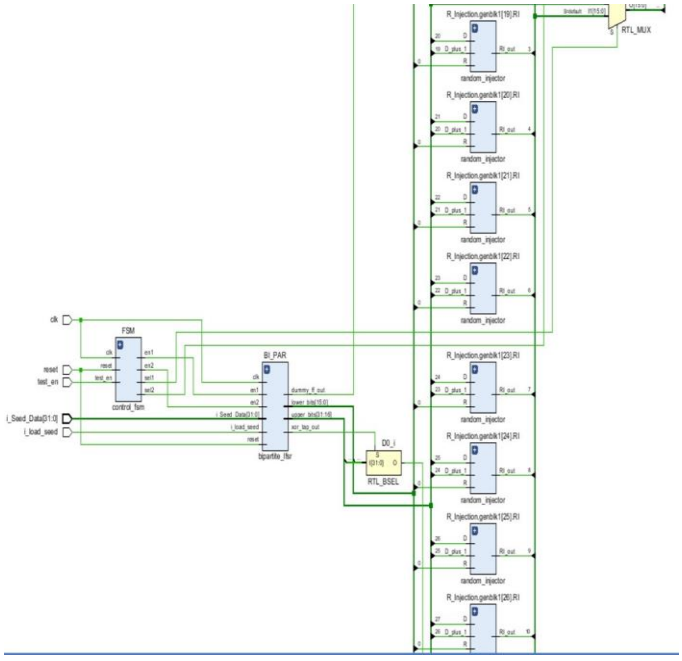

Figure.3 LT-LFSR

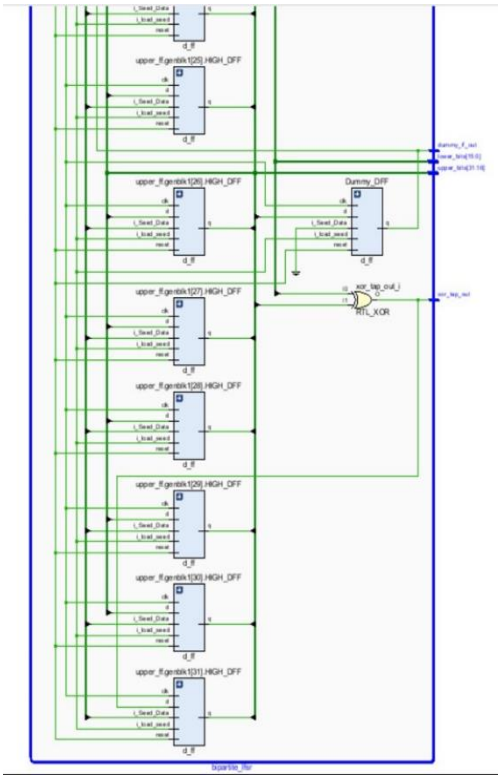

Figure.4 BI-Pirate

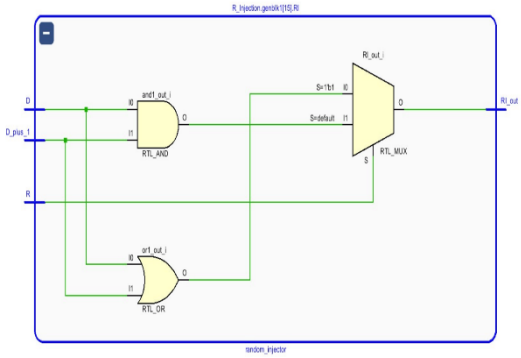

Figure.5 Random Injection Area Report

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	132	0	303600	0.04
LUT as Logic	132	0	303600	0.04
LUT as Memory	0	0	130800	0.00
Slice Registers	103	0	607200	0.02
Register as Flip Flop	71	0	607200	0.01
Register as Latch	32	0	607200	<0.01
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
LUT3	96	LUT
IBUF	36	IO
FDCE	35	Flop & Latch
OBUF	32	IO
LUT6	32	LUT
LDCE	32	Flop & Latch
FDPE	32	Flop & Latch
LUT2	6	LUT
BUFG	3	Clock
FDSE	2	Flop & Latch
FDRE	2	Flop & Latch
LUT1	1	LUT

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ADVANTAGES

Reduced power consumption: LPTPGs are specifically designed to generate test patterns that consume less power compared to traditional test pattern generators. This means that LPTPGs are ideal for testing low-power circuits, such as those found in portable electronic devices.

Faster testing: LPTPGs can generate test patterns much faster than traditional test pattern generators, which means that they can speed up the testing process and reduce overall testing time.

Improved accuracy: LPTPGs can generate test patterns with greater accuracy, which means that they can help identify problems in circuits more effectively. This is particularly important in complex circuits where identifying problems can be challenging.

Cost-effective: LPTPGs can be less expensive than traditional test pattern generators, which means that they can be an affordable option for companies that need to test a large number of

APPLICATIONS

Mobile devices: LPTPGs are ideal for testing the low-power circuits found in mobile devices, such as smartphones, tablets, and wearables. These devices require long battery life, and LPTPGs can generate test patterns that consume less power, which is important for preserving battery life.

Internet of Things (IoT): LPTPGs are also commonly used in the testing of IoT devices, which often have low-power requirements due to their limited power sources, such as batteries. LPTPGs can generate test patterns that are specifically designed for low-power IoT devices, which can help ensure that these devices function correctly and efficiently.

Automotive electronics: LPTPGs are used to test the electronic systems in automobiles, such as engine management systems and advanced driver assistance systems (ADAS). These systems have strict power requirements, and LPTPGs can help ensure that they operate correctly while minimizing power consumption.

Aerospace and defence: LPTPGs are used to test the electronic systems in aerospace and defence applications, such as aircraft control systems and missile guidance systems. These

systems have strict power requirements and must operate reliably in harsh environments, making LPTPGs an essential tool for testing and verification.

CONCLUSION

This project shows an effective HDL implementation of low power utilization for test pattern generator using the Low Power LFSR technique. It also addresses a theory to express a test pattern creation by using Low Transition Linear Feedback Shift Register architecture. By using this technique; power consumption can be reduced as compared to the conventional LFSR technique. It shows that the total power consumed in low transition linear feedback shift register is 50.06% less than the conventional LFSR. From the results, it shows that Low Power LFSR is very much constructive for power reduction techniques during testing mode.

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