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AREA AND DELAY EFFICIENT AOI AND OAI BASED FULL ADDER FOR RCA

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ABSTRACT

In this Project critical path of ripple carry adder (RCA)-based binary tree adder (BTA) is analyzed to find the possibilities for delay minimization. Based on the findings of the analysis, the new logic formulation and the corresponding design of RCA are proposed for the BTA. The comparison results shows that the proposed RCA design offers better efficiency in terms of area, delay and energy than the existing RCA. Using this RCA design, the BTA structure is proposed and therefore, the proposed BTA design can be a better choice to develop the area, delay and energy efficient digital systems for signal and image processing applications,

INTRODUCTION

In the rapidly advancing landscape of digital circuit design, the quest for achieving optimal balance between area and delay efficiency has become imperative. This document introduces a groundbreaking approach in the form of the Area and Delay Efficient AOI (AND-OR-Invert) and OAI (OR-AND-Invert) Based Full Adder, specifically tailored for Ripple Carry Adder (RCA) applications. Traditional Full Adder designs have faced challenges related to area consumption and propagation delay, prompting the exploration of innovative solutions. By harnessing the capabilities of the compact AND-OR-Invert (AOI) and OR-AND-Invert (OAI) gates, this Full Adder design not only addresses these challenges but also presents a versatile and high-performing solution. This document aims to elucidate the advantages, applications, and implications of this novel approach, shedding light on its potential to reshape the landscape of digital circuitry.

In the ever-evolving realm of semiconductor technologies, where the demand for smaller, faster, and more energy-efficient systems is relentless, the proposed AOI and OAI based Full Adder emerges as a promising solution. This innovative design seeks to redefine the traditional

trade-offs between speed and compactness. The incorporation of AOI and OAI gates not only achieves a remarkable reduction in transistor count but also significantly minimizes propagation delays, leading to a Full Adder design that strikes an optimal balance between area efficiency and speed.

LITERATURE SURVEY

1."An area-delay efficient multi-operand binary tree adder using modified carry select adder" by M. Singh, M. Sharma, and A. K. Verma (2016):

This paper proposes an area-delay efficient MOBTA that uses a modified carry select adder (MCSA) as the building block. The proposed adder is shown to have a smaller area and delay than other existing MOBTAs while still maintaining a similar power consumption.

2. "Low power and high-speed multi-operand binary tree adder" by A. Mittal, M. Gupta, and R. S. Anand (2017):

This paper proposes a low-power and high-speed MOBTA that reduces power consumption by optimizing the carry propagation path and reducing the number of logic gates required to implement the adder. The proposed adder is shown to have a lower power consumption and a faster speed than other existing MOBTAs.

3. "Low-Power Multi-Operand Binary Tree Adder Design Based on Signed-Digit Number System" by C. Li, Y. Li, and J. Li (2019):

This paper proposes a low-power MOBTA design based on the signed-digit number system (SDNS). The proposed design reduces power consumption by exploiting the redundancy in the SDNS representation and using a carry-save adder (CSA) as the building block.

4. "Design of low-power multi-operand binary tree adder using hybrid binary adder cells" by S. Patra, S. Pal, and D. K. Mandal (2020):

This paper proposes a low-power MOBTA design using hybrid binary adder cells (HBACs). The proposed design reduces power consumption by optimizing the carry propagation path and reducing the number of logic gates required to implement the adder.

5. "Design of an efficient multi-operand binary tree adder for high-performance arithmetic circuits" by H. Farrahi and S. M. Fakhraie (2020):

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This paper proposes an efficient MOBTA design that reduces delay and power consumption by using a modified Kogge-Stone adder (MKSA) as the building block. The proposed adder is shown to have a lower delay and power consumption than other existing MOBTAs.

PROPOSED METHODOLOGY

The two 1-bit logic cells (AOI-LC and OAI-LC) are derived using the proposed logic formulation given above, and shown in Fig. below. The AOI-LC takes inputs ai, bi and ci - 1, and computes sum (si) and intermediate carry-out ci signals while the OAI-LC computes sum (si) and carry-out (ci) signals using 1-bit input signals ai, bi and ci - 1.

Using AOI-LC and OAI-LC modules, an m-bit RCA design is proposed as shown in Fig.. In the proposed RCA design, the AOI-LC and OAI-LC modules are connected alternatively because AOI-LC generates carry-out in the complement form while the OAI-LC generates normal carry-out. It takes m-bit inputs (a and b) and initial carry-in (cin) to compute the sum (s) and carry-out cout signals, where the output carry is equal to cm - 1. If the value of m is odd then the proposed RCA includes AOI-LC in the MSB bit position which generates the carry-out signal in the complement form. Therefore, an actual output carry is obtained by complementing the carry-out signal of the AOI-LC placed in the MSB position.

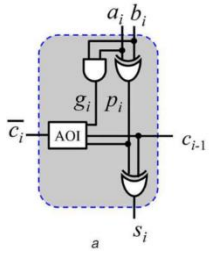

Figure.1 Generalized AOI

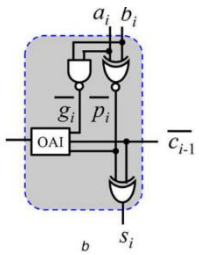

Figure.2 Generalized OAI

Logic formulation and proposed RCA design:

The objective of this logic formulation is to compute the intermediate carry signals using AOI gates for the minimization of the carry propagation delay of RCA. Hence, the carry expression is expressed in the AOI form as

$$\overline{c_i} = \underbrace{\overline{g_i + p_i \cdot c_{i-1}}}_{\text{AOI}}$$

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The ith carry signal computed is in complement form and cannot be directly used to compute the (i + 1)th carry signal. Therefore, the expression of valid (i + 1)th carry signal using the ith carry ci is given as

$$c_{i+1} = \underbrace{\overline{g_{i+1} \cdot (\overline{p_{i+1}} + \overline{c_i})}}_{\text{OAI}}$$

The operation given can be performed by using an OAI complementary gate which produces carry ci + 1 signal in the normal form. However, it is clear that the OAI-based carry computation requires pi + 1, gi + 1 and ci signals in their complemented form. Therefore, based on these observations, the new logic formulation for the RCA design which favours the AOI/OAI-based realization of the carry generation is given as:

(i) Boolean expressions with AOI-based carry generation:

$$p_i = a_i \oplus b_i; \quad g_i = a_i \cdot b_i$$

$$\overline{c_i} = \overline{g_i + p_i \cdot c_{i-1}}$$

$$s_i = p_i \oplus c_{i-1}$$

(ii) Boolean expressions with OAI-based carry generation:

$$\overline{p_i} = \overline{a_i \oplus b_i}; \quad \overline{g_i} = \overline{a_i \cdot b_i}$$

$$c_i = \overline{\overline{g_i} \cdot (\overline{p_i} + \overline{c_{i-1}})}$$

$$s_i = \overline{p_i} \oplus \overline{c_{i-1}}$$

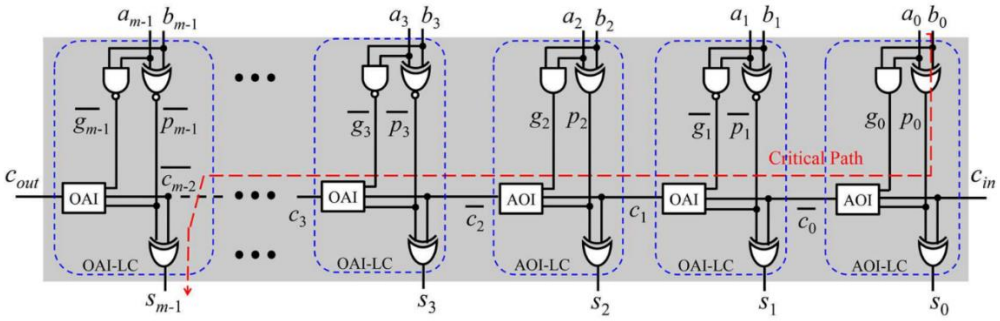

Figure.3 Proposed m-bit RCA design

SIMULATION & SYNTHESIS RESULTS

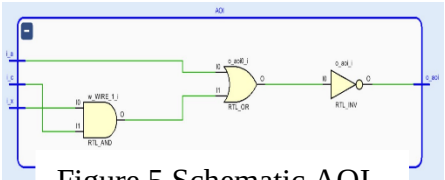

Figure.5 Schematic AOI

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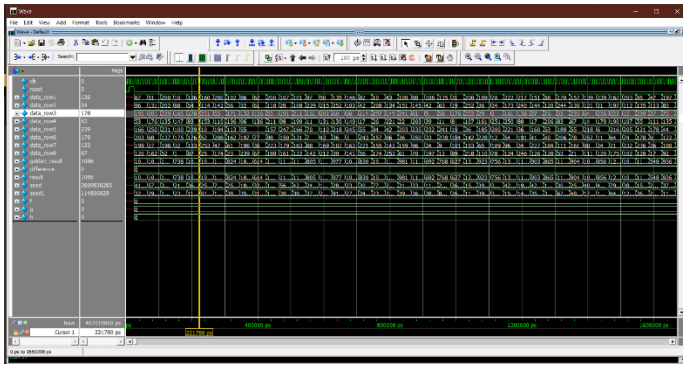

Figure.4 Simulation Wave 1

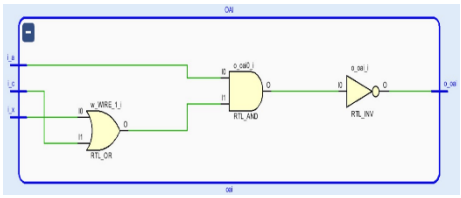

Figure.6 Schematic OAI

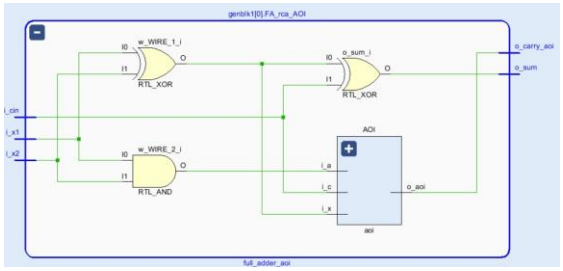

Figure.7 Schematic Full Adder AOI

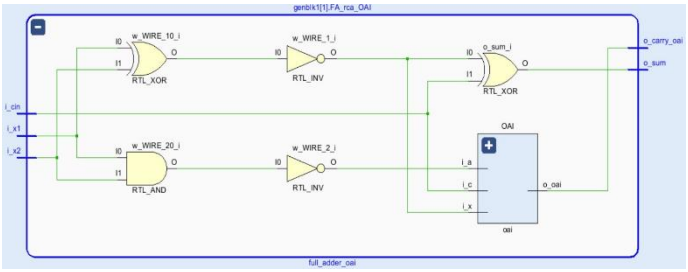

Figure.8 Schematic Ful Adder OAI

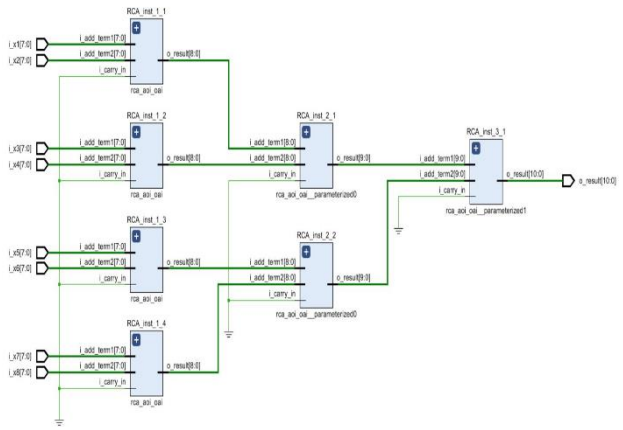

Figure.9 Schematic Added Tree

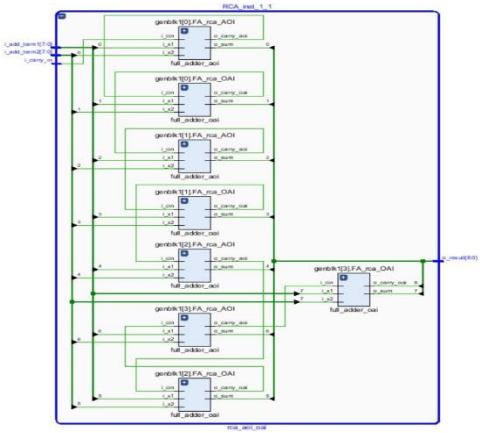

Figure.10 Schematic RCA

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	67	0	303600	0.02
LUT as Logic	67	0	303600	0.02
LUT as Memory	0	0	130800	0.00
Slice Registers	0	0	607200	0.00
Register as Flip Flop	0	0	607200	0.00
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Ref Name	Used	Functional Category
IBUF	64	IO
LUT5	33	LUT
LUT6	28	LUT
LUT3	14	LUT
OBUF	11	IO
LUT4	10	LUT
LUT2	3	LUT

Figure.11 Area Report

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ADVANTAGES

Reduced Area: Multi-operand binary tree adders have a smaller area compared to other types of adders. This is because the binary tree structure reduces the number of full adders required to add multiple numbers together.

Reduced Delay: Multi-operand binary tree adders have a shorter propagation delay compared to other types of adders. This is because the binary tree structure allows the carry signals to propagate in parallel, reducing the critical path delay.

Reduced Power Consumption: Multi-operand binary tree adders have a lower power consumption compared to other types of adders. This is because the binary tree structure allows the carry signals to propagate in parallel, reducing the overall power consumption.

Scalability: Multi-operand binary tree adders are highly scalable. They can easily be expanded to add more numbers by adding more stages to the binary tree structure. This makes them suitable for a wide range of applications where the number of operands may vary.

APPLICATIONS

Multi-precision arithmetic: multi-operand binary tree adders are used to perform addition operations on numbers with multiple digits, such as in cryptography, numerical simulations, and financial applications.

Image and video processing: Efficient multi-operand binary tree adders can be used to perform fast pixel-level operations on images and videos, such as in image filtering and compression algorithms.

Digital signal processing: Efficient multi-operand binary tree adders are used in DSP applications, such as in FIR and IIR filters, discrete cosine transform (DCT), and FFT algorithms.

Machine learning: Multi-operand binary tree adders can be used to implement fast matrix operations in machine learning algorithms, such as in neural networks.

CONCLUSION

The RCA-based BTA is widely used MOA (Multi Operand Adder) due to its simplest structure that leads to area and energy efficient design. However, the long carry propagation path of

RCA makes it poor in terms of delay performance. Therefore, in this paper, the delay analysis of RCA-based BTA is presented. Based on the analysis, the new logic formulation for RCA using complementary logic operations is derived and correspondingly the RCA design is proposed for the BTA. The comparison result shows that the proposed RCA provides better efficiency in terms of area, delay and energy than the existing RCA. Using this RCA design, the BTA structure is proposed. The synthesis result reveals that the proposed 8-operand BTA provides the saving of 22.5% in area over existing AT available MOAs.

FUTURE SCOPE

Hardware Design: Binary adder trees are commonly used in the design of digital circuits, such as processors, to perform arithmetic operations. As the demand for faster and more efficient processors continues to grow, the use of binary adder trees in hardware design is likely to increase.

Cryptography: In cryptography, binary adder trees are used to perform modular arithmetic, which is a fundamental operation in many cryptographic algorithms. The use of binary adder trees in cryptography is likely to increase as the need for secure and efficient encryption methods continues to grow.

Big Data Processing: With the exponential growth of data in recent years, the need for fast and efficient data processing methods has become more critical than ever. Binary adder trees can be used to perform fast parallel addition operations on large datasets, making them useful in big data processing applications.

REFERENCES

[1] Jiang, H., Liu, L., Jonker, P.P., et al.: ‘A high-performance and energy efficient FIR adaptive filter using approximate distributed arithmetic circuits’, IEEE Trans. Circuits Syst. I, Regul. Pap., 2018, 66, (1), pp. 313–326

[2] Mittal, A., Nandi, A., Yadav, D.: ‘Comparative study of 16-order FIR filter design using different multiplication techniques’, IET Circuits Devices Syst., 2017, 11, (3), pp. 196–200

[3] Tang, Z., Zhang, J., Min, H.: ‘A high-speed, programmable, CSD coefficient FIR filter’, IEEE Trans. Consum. Electron., 2002, 48, (4), pp. 834–837

ISSN2454-9940

www.ijsem.org

Vol 18, Issuse.1 March 2024

[4] Chen, K.H., Chiueh, T.D.: 'A low-power digit-based reconfigurable FIR filter', IEEE Trans Circuits Syst. II, Express Briefs, 2006, 53, (8), pp. 617–621

[5] Mohanty, B.K., Patel, S.K.: 'Efficient very large-scale integration architecture for variable length block least mean square adaptive filter', IET Signal Process., 2015, 9, (8), pp. 605–610

[6] Meher, P.K.: 'Seamless pipelining of DSP circuits', Circuits Syst. Signal Process., 2016, 35, (4), pp. 1147–1162

[7] Behrooz, P.: 'Computer arithmetic: algorithms and hardware designs' (Oxford University Press, USA, 2000)