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Design of Reversible Decoder with MOS Transistors for Low-Power and Fault Tolerance

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Abstract: The approach adopted for this design centers around reversible logic synthesis, specifically tailored for the creation of an n-to-2n decoder, with 'n' signifying the quantity of data bits. In this context, the circuitry is exclusively structured utilizing reversible, fault-tolerant Fredkin and Feynman double gates. Consequently, the entire system inherently possesses fault tolerance as an integral feature. Furthermore, the paper encompasses an algorithm devised for the purpose of crafting this generalized decoder, ensuring versatility in its applicability. Additionally, the study introduces several lower bounds pertaining to constant inputs, garbage outputs, and the quantum cost associated with the reversible, fault-tolerant decoder. The comparative analysis undertaken reveals the superiority of the proposed design across various dimensions, including quantum cost, delay, hardware complexity, and scalability, significantly outperforming existing methodologies.

Index Terms— Reversible Decoder, High speed, MOS Transistor, low power.

INTRODUCTION

VLSI signifies "Incredibly Large Scale Integration". This is the field that incorporates squeezing progressively more reasoning contraptions into progressively little areas. VLSI, circuits that would have taken boards of space can now be put into a little space relatively few millimeters across! This has opened up a significant entryway to do things that were illogical beforehand. VLSI circuits are everywhere .your PC, your vehicle, your crisp out of the plastic new state-of-the-art progressed camera, the cells, and what have you. This remembers a lot of expertise for some fronts inside the comparative field, which we will look at in later regions. VLSI has been around for a long time, but because of advances in the domain of PCs, there has been a shocking increase in devices that can be used to arrange VLSI circuits. Nearby, consenting to Moore's guideline, the limit of an IC has extended drastically all through the long haul, to the extent that estimation power, utilization of available area, yield. The united effect of these two advances is that people can now put different helpfulness into the Ic's, opening up new edges. Models are introduced systems, where brilliant contraptions are put inside conventional things, and ubiquitous figuring where little enrolling devices duplicate such a lot of that even the shoes you wear may truly achieve something accommodating like noticing your heartbeats. Consolidated

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circuit (IC) development is the engaging advancement for a whole host of innovative devices and systems that have changed the way wherein we live. Jack Kilby and Robert Noyce got the 2000 Nobel Prize in Physics for their formation of the organized circuit; without the consolidated circuit, neither semiconductors nor PCs would be anyway critical as they appear to be today. VLSI systems are significantly more humble and consume less power than the discrete parts used to develop electronic structures before the 1960s. Compromise licenses us to build systems with significantly more semiconductors, allowing considerably seriously handling capacity to be applied to handling an issue. Composed circuits are similarly significantly more direct to plan and deliver and are more strong than discrete systems; that makes it possible to encourage specific explanation structures that are more viable than extensively valuable PCs for the principle work.

1.1 ADVANTAGES OF VLSI

While we will zero in on composing circuits in this book, the properties of consolidated circuits that we can and can't put in a fused circuit generally choose the plan of the entire system. Facilitated circuits further foster structure characteristics in a greater number of ways than one. I appreciate three basic high grounds over automated circuits worked from discrete parts:

• Size. Composed circuits are much more unobtrusive the two semiconductors and wires are contracted to micrometer sizes, standing out from the millimeter or centimeter sizes of discrete parts. Little size prompts benefits in speed and power use since more unobtrusive parts have more unassuming parasitic assurances, capacitances, and inductances.

• Speed. Signs can be traded between reasoning 0 and reasoning 1 a lot quicker inside a chip than they can between chips. Correspondence inside a chip can happen commonly faster than correspondence between chips on a printed circuit load up. The high speed of circuits on-chip is a result of their little size-more unassuming parts and wires have more humble parasitic capacitances to tone down the transmission.

• Power usage. Reasoning errands inside a chip similarly take extensively less power. Once lower power usage is generally a direct result of the little size of circuits on the chip-more unobtrusive parasitic capacitances and securities require less capacity to drive them.

1.2. ROUTING

The arranging framework picks the specific ways for interconnections. This merges the standard cell and gigantic expansion sticks, the pins on very far or pads past what many would think about conceivable. After a strategy and CTS, the instrument has information about the particular areas of squares, pins of squares, and I/O pads at chip limits. The expected relationship as portrayed by the netlist is furthermore open to the mechanical social affair. In the getting sorted out stage, metal and vias are used to make the electrical relationship in arrangement to complete all affiliations portrayed by the netlist. Now, to do the authentic interconnections, the contraption relies on some "Plan Rules".

Most of the switches open are network-based switches. There are arranging lattices portrayed for the entire course of action. Consider it as a plan as under. For structure-based switches, there are moreover preferred controlling headings portrayed for each metal layer. for instance, Metal1 has an inclined in the direction of the course of "level', metal2 has truly leaned toward coordinating heading of "vertical, and so on Along these lines, in the whole course of action, metal1 arranging affiliations will be drawn (superimposed) on a level plane with metal1 wire pitch and metal2 cross-regions will be drawn vertical with metal2 wire pitch between each.

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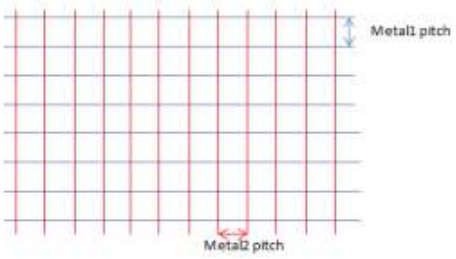

Figure 1 : Routing Grids

The above figure shows how coordinating grids are drawn. Here only two metals are considered for the present, but in a cycle with more metals, relative structures will be superimposed on the organization for each available metal. Not entirely settled by concluding the base scattering expected between system lines of the same metal.

This can be the base scattering of the metal but is by and large a value more imperative than the base isolating. Not set in stone by considering the through viewpoint additionally, with the objective that no two connecting wires on the cross-section make any DRC encroachment regardless when there are vias present.

2. Experience and Assessment:

Our transitory work range was of a half year. Immediately when we started, classes were coordinated and I acquired various thoughts as indicated by present-day viewpoint and liked them executing all things considered. Then, our affiliation had embraced projects from St. Mary's school, Hyderabad, a piece of those errands were done by me and I went to the show in that school and connected with students for our affiliation.

The inclusion with the association was pleasant, people work in co-arrangement and the association environment is especially safeguarded and studios. The inspiration to pick this association was that it was offering section level situation in VLSI which is my middle specialization in PG degree and I expected to benefit from this experience, in like manner I got to learn new instruments like Electric, Symica DE, and Microwind.

I used to spend just about 5 to 6 hours consistently in the association offering a chance with different circuits and making their arrangements genuinely. I thank my helper who was, by and large, there nearby all through my brief work process offering me direction, information, and tips on how people work in an industrial environment.

A couple of specific outcomes are:

VLSI chip's application is for the most part for mobile phones which are dependent upon having a longer battery span. Likewise, the new electronic things require extended value, first-class execution, and coordination of a colossal number of parts inside a lone chip provoking power-consumed plans. So how to make the chip lower power is essential for the association.
The goals of a chipmaker are:

- To reduce power use.
- To lessen district.
- To accelerate and execution of the chip.

A couple of non-specific outcomes are:

- The assurance level is extended.
- Stage fear vanishes.
- I have encouraged the ability to explain my viewpoint to the front individual clearly.
- I discovered how things will be finished in a certified industry.

4.2 Contribution to the Organization:

During my brief work, I expected to add to the association's endeavors by applying the data which I have procured during my entry-level position learning process. So I have contributed by arranging a low power-area capable 1 digit full snake using the gadget Microwind2.

3. REVERSIBLE LOGIC GATES

Reversible logic plays a crucial role in low-power computing due to its ability to recover from bit loss through a unique mapping between input and output vectors. This property of reversible circuits significantly reduces power dissipation compared to conventional circuits. Additionally, reversible logic is considered a subset of quantum circuits

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since quantum evolution must inherently be reversible. Over the past two decades, reversible circuitry has garnered substantial interest in various fields, including DNA technology, nanotechnology, optical computing, program debugging and testing, quantum dot cellular automata, discrete event simulation, and the development of highly efficient algorithms.

Parity checking is a widely used mechanism for detecting single-level faults. When the parity of input data is consistently maintained throughout computation, the need for intermediate checking is reduced. An entire circuit can preserve parity if its individual gates are parity-preserving. Reversible fault-tolerant circuits, built using fault-tolerant gates, enable the detection of faulty signals in the primary outputs through parity checking.

The hardware of digital communication systems heavily relies on decoders to retrieve information from coded outputs. Decoders are also integral components in the memory and I/O systems of microprocessors. While a reversible fault-tolerant decoder was designed in a previous study, it lacked generalization and compactness. Therefore, this research focuses on exploring generalized design methodologies for reversible fault-tolerant decoders.

BASIC CONCEPTS

This section formally introduces the concepts of reversible gates, garbage outputs, delay, hardware complexity, and presents well-known reversible fault-tolerant gates, along with their input-output specifications, transistor representations, and quantum equivalents.

A. Reversible and Fault Tolerant Gates

An n×n reversible gate serves as a data stripe block that uniquely establishes a mapping between an input vector, denoted as Iv = (I0, I1, ..., In−1), and an output vector, Ov = (O0, O1, . . . , On−1), symbolized as Iv ↔ Ov. Two fundamental prerequisites for a reversible logic circuit are as follows: • An equal number of inputs and outputs must be present.

A fault-tolerant gate is a reversible gate that consistently upholds the same parity between the input and output vectors. More precisely, an n × n fault-tolerant gate is characterized by the following property between the input and output vectors [2]:

$I0 \oplus I1 \oplus ... \oplus In-1 = O0 \oplus O1 \oplus ... \oplus On-1$ (1)

The property of preserving parity, as indicated in Equation 1, enables the detection of a faulty signal at the primary output of the circuit. Researchers [2] have demonstrated that a circuit composed solely of reversible fault-tolerant gates can maintain parity, thereby facilitating the detection of faulty signals at its primary output.

B. Qubit and Quantum Cost

The fundamental distinction between qubits and conventional bits lies in the fact that qubits can form linear combinations of states $|0\rangle$ or $|1\rangle$, a property known as superposition, whereas the basic states $|0\rangle$ or $|1\rangle$ represent an orthogonal basis of a two-dimensional complex vector space. Superposition can be expressed as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$, signifying that the probability of measuring a particle in state 0 is $|\alpha|2$, and it yields the result 1 with probability $|\beta|2$, with the constraint $|\alpha|2 + |\beta|2 = 1$. Consequently, the information stored in a qubit varies depending on the values of α and β. This unique property enables qubits to perform certain computations exponentially faster than conventional bits, which serves as a primary motivation for quantum computing.

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Quantum computers necessitate that their underlying circuitry be reversible.

C. Delay, Garbage Output, and Hardware Complexity

The delay of a circuit corresponds to the delay of its critical path. The critical path is defined as the path with the maximum number of gates connecting any input to any output. A circuit may have multiple critical paths, and identifying all of them is an NP-complete problem. Consequently, researchers typically focus on the path that is most likely to be the critical path.

Garbage output in a reversible gate (or circuit) refers to outputs that are only required to maintain reversibility. These outputs are considered extraneous and have no meaningful function beyond this requirement.

Hardware complexity for a circuit is determined by the number of basic operations (e.g., Ex-OR, AND, NOT) necessary for its realization.

Experience and Assessment

My experience at the company was highly satisfactory. People at the company work in a coordinated manner, and the work environment is safe and conducive to learning. I chose this company for my internship because it offered opportunities in VLSI, which aligns with my core specialization in my PG degree. I was eager to gain practical experience and learn to use new tools such as Electric, Symica, and Microwind.

I dedicated approximately 5 to 6 hours each day at the company, experimenting with different circuits and manually creating their layouts. I am deeply grateful to my guide, who provided unwavering support throughout my internship, offering valuable advice, feedback, and insights into how the industry operates.

Some of the technical outcomes of my internship include a deeper understanding of VLSI chip applications, particularly in the context of mobile devices where power efficiency is crucial. As electronic products continue to demand increased functionality and integration of numerous components within a single chip, the challenge lies in designing power-efficient solutions. The primary goals for a chip manufacturer are to reduce power consumption, minimize chip area, and enhance chip speed and overall performance.

On the non-technical side, my confidence levels have significantly increased, and any stage fright I had previously experienced has largely disappeared. I have developed the ability to articulate my thoughts and perspectives clearly, which is a valuable skill in any professional setting. Additionally, I gained valuable insights into how operations are carried out in a real industry environment.

Scope of Work

During my internship, I aimed to actively contribute to the company's projects by applying the knowledge I had acquired throughout my internship learning process. As a result, I worked on the Design of Reversible Decoder with MOS Transistors for Low-Power and Fault Tolerance with the assistance of the Microwind tool.

Microwind is a free open-source EDA (Electronic Design Automation) system that offers a range of services, including IC layout handling, schematic drawing, textual hardware description language support, and more. This software simplifies the design of micrometer-sized ICs by providing various features for IC layout design and verification. MicroWind VLSI Design System facilitates the systematic and efficient design of schematics and layouts,

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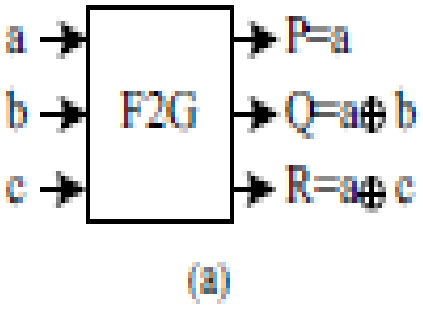
ultimately saving time and reducing production costs for IC chips.

In my implementation, I utilized CMOS technology due to its scalability, high noise immunity, and low power consumption. CMOS technology employs both NMOS and PMOS transistors, ensuring that only one type of transistor is active at any given time during operation. This characteristic results in reduced power consumption, as power is utilized only when the transistors switch between on and off states.

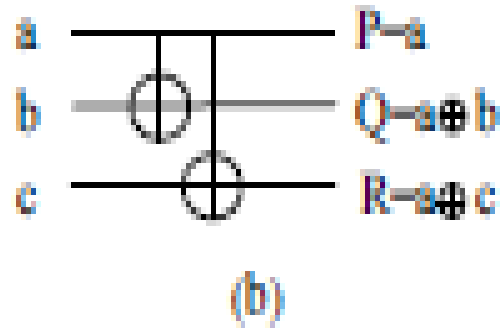
Popular Reversible Fault Tolerant Gates

1. **Feynman Double Gate**:

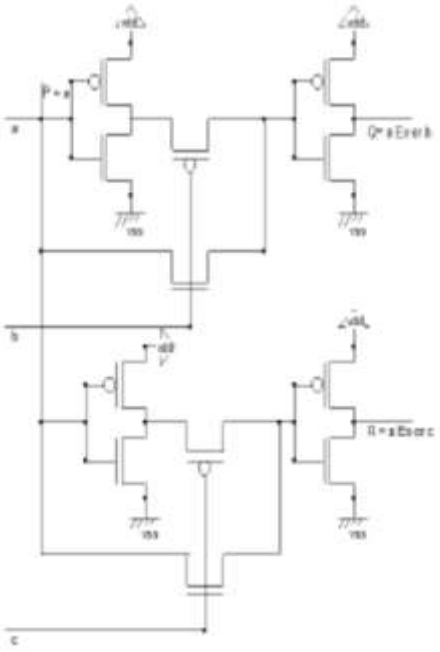
The input vector (Iv) and output vector (Ov) for a 3×3 reversible Feynman double gate (F2G) are defined as follows: Iv = (a, b, c) and Ov = (a, a ⊕ b, a ⊕ c). The block diagram of F2G is depicted in Fig. 4.3.1(a). Fig. 4.3.1(b) illustrates the quantum equivalent realization of F2G, which shows that it is constructed using two 2×2 Ex-OR gates, resulting in a quantum cost of two. In accordance with our design procedure, F2G requires twelve transistors to achieve reversible functionality, as shown in Fig. 4.3.1(c). The corresponding timing diagram for F2G is presented in Fig. 4.3.9(a), while Fig. 4.3.2 displays the schematic of F2G in Microwind, and its layout is shown in Fig. 4.3.3, with the simulated schematic depicted in Fig. 4.3.4.



(a)



(b)



(c)

Fig.4.3.1: Reversible Feynman double gate (a) Block diagram (b) Quantum equivalent realization (c) Transistor realization

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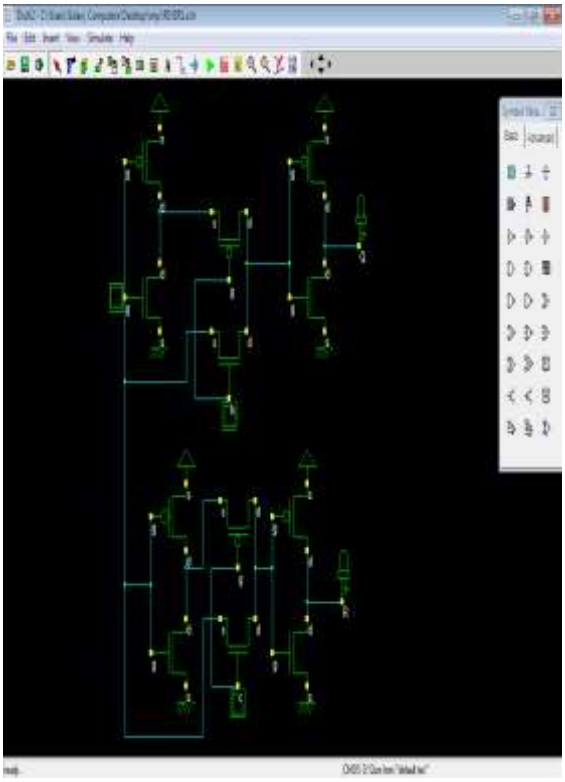

Fig.4.3.2: schematic of Feynman double gate

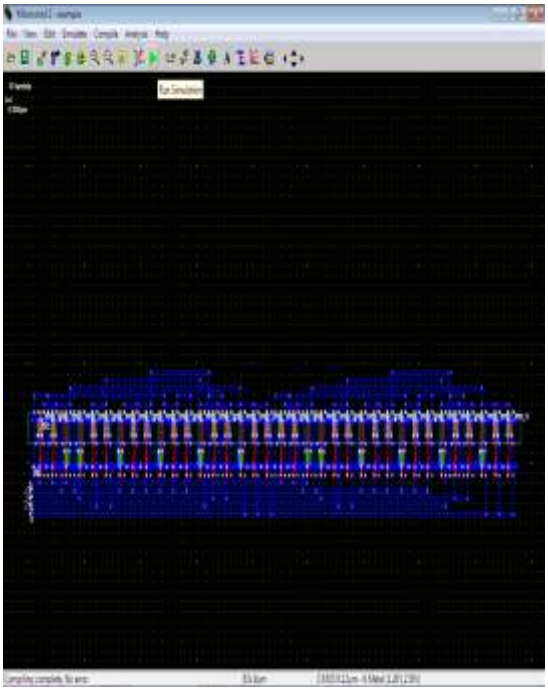

Fig.4.3.3: Layout of Feynman double gate

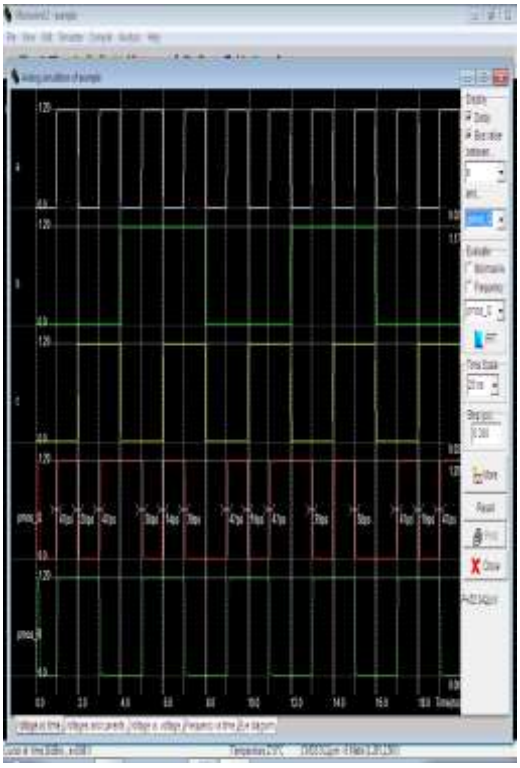

Fig.4.3.4:Graph of Feynman double gate

6. Conclusion and Future Work

In this study, we have elucidated the design principles of an n-to-2n reversible fault-tolerant decoder, with n representing the number of data bits. Our contributions encompass the introduction of various lower bounds related to the quantities of garbage outputs, constant inputs, and quantum cost. We have substantiated that the proposed circuit has been structured with the optimal arrangement of garbage outputs, constant inputs, and quantum cost.

Additionally, we have delineated the blueprints for the constituent gates of the decoder, employing MOS transistors to facilitate the implementation of the decoder's circuit with transistors. Through simulations of the transistor-based implementation of the decoder, we

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have validated the flawless functionality of the proposed fault-tolerant decoder. Comparative assessments have demonstrated the superior performance of our designs compared to their counterparts. We have buttressed the effectiveness and supremacy of our proposed approach with robust theoretical justifications.

These reversible fault-tolerant decoders hold the potential for deployment in diverse applications, including parallel circuits, multiple-symbol differential detection, network components, and digital signal processing, among others.

REFERENCES

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "New security systems against SEUs for moving typical diverts in a radiation environment," IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 957-964, Aug. 2007.

[2] M. Hatamian et al., "Plan examinations for gigabit ethernet 1000 base-T reshaped pair handsets," Proc. IEEE Custom Integr. Circuits Conf., pp. 335-342, 1998.

[3] H. Yamasaki and T. Shibata, "A consistent picture feature extraction and vector-age VLSI using showed shift-register designing," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046-2053, Sep. 2007.

[4] H.- S. Kim, J.- H. Yang, S.- H. Park, S.- T. Ryu, and G.- H. Cho, "A 10-digit section driver IC with parasitic-inhumane iterative charge-sharing based capacitor-string inclusion for flexible powerful lattice LCDs," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766-782, Mar. 2014.

[5] S.- H. W. Chiang and S. Kleinfelder, "Scaling and plan of a 16-megapixel CMOS picture sensor for electron microscopy," in Proc. IEEE Nucl. Sci. Symp. Conf. Record (NSS/MIC), 2009, pp. 1249-1256.

[6] S. Heo, R. Krashinsky, and K. Asanovic, "Activity fragile flip-flop moreover lock assurance for decreased energy," IEEE Trans. Extraordinarily Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060-1064, Sep. 2007.

[7] S. Naffziger and G. Hammond, "The execution of the next-generation 64 b Itanium chip," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276-504.

[8] H. Partovi et al., "Course through lock and edge-set off flip-flop cream parts," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 138-139, Feb. 1996.

[9] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Unexpected push-pull beat snare with 726 flops energy concede thing in 65 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482-483.

[10] V. Stojanovic and V. Oklobdzija, "Comparable assessment of master-slave snares and flip-flops for predominant execution and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536-548, Apr. 1999.