ISSN: 2454-9940

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

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INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940www.ijsem.in

Vol 9, Issuse.4 Dec 2021

Design and Implementation of Current-Mode Clock Synthesis CMCS

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ABSTRACT:
VLSI clock networks are power hogs because of how much processing power they demand. Because of the enormous global clock capacitance, voltage-mode (VM) signaling is used by most current techniques, however this results in a significant loss of dynamic power. Current-mode (CM) clocking methods have been confined to just symmetric networks, but most application-specific integrated circuits (ASICs) have symmetric clock distributions. CM clock synthesis (CMCS) is proposed in this research to minimize total clock network power while maintaining minimal skew. Traditional clock routing and transmitter and receiver sizes may be used in conjunction with this strategy. SPICE models generated from ISPD 2009 and 2010 industry benchmarks are used to test the suggested technique. Using 45-nm CMOS technology, this strategy decreases the average power with a comparable skew on the benchmarks.

EXISTINGMETHOD:
Different approaches to reducing CDN power have previously been offered by many academics Besides power, a lot of research has been done on signal integrity difficulties. duetoprocessvariationandnoise.Researchersm ostlyimprovedtheseattributesconsidering apowerbudgetasaprimary constraint. All of the CDN efforts toimprovesignalintegrityandpowerarebasedo ntraditionalvoltagemode(VM)signaling.

PROPOSEDMETHOD:
Distributed buffers are not required for a current-mode (CM) signal, which reduces the variability of the process and noise-related timing errors. With its low voltage wing, CM signaling is able to transmit more quickly than VM signaling, which has lower dynamic power. Our suggested solution is the first to distribute CM clock signals in actual clock networks utilizing a standard-cell design style. The following is a list of our main contributions:
Clock synthesis technology to construct non-symmetric Clock CM clocks; CM clocking demonstration using industry benchmarks;
3) The first standard-cell approach to decrease skew by using CM latch/flip-flop input impedance.

I.INTRODUCTION
CDN power may be reduced by several methods offered by researchers. More than just energy is being spent on signal integrity, which is affected by process variation and noise. Researchers primarily enhanced these characteristics while keeping an eye on their power budget. Traditional voltage-mode (VM) signaling is used in all CDN initiatives to increase signal integrity and power. Low-voltage swing signaling, differential signaling, pseudo-differential signaling, and incremental

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signaling have all been studied as an extension of VM signaling. Only non-clock signals could be sent by the latter two schemes; yet, they outperformed the full l swing VM methods in terms of power and performance. There are VM CDNs that need buffers, but the location of these buffers may disrupt timing and require enhanced clock syn-thesis techniques to address skew and unpredictability. Instead of using buffers, a current-mode (CM) signal reduces process variance as well as noise-related timing errors. When compared to VM signaling, CM signaling has a faster transmission speed and a lower dynamic power because to its lower voltage swing. As a further benefit, CM signaling has lower switching and substrate noise than VM methods, while also providing improved signal integrity.

Our suggested solution is the first to distribute CM clock signals in actual clock networks utilizing a standard-cell design style. The following is a list of our main contributions: Nonsymmetric CM clock synthesis was pioneered using this technology.

clocks;2)thefirstdemonstrationofCMclockingo nindustrialbenchmarks;3)thefirststandard-cellmethodologytoutilizeCMlatch/flip-flopinputimpedancetominimizeskew.

BACKGROUND

Global signaling, notably high-speed serial communications for network buses, memory buses, and multiprocessor interconnection networks, is extensively employed in CM technology. Low-frequency CM signaling, on the other hand, uses a lot of power because of the high use of static power. CMOS logic, on the other hand, relies on VM signaling because to the lower static power. It's been proven that CMOS current steering logic is resistant to digital switching noise, but static power consumption is too high.

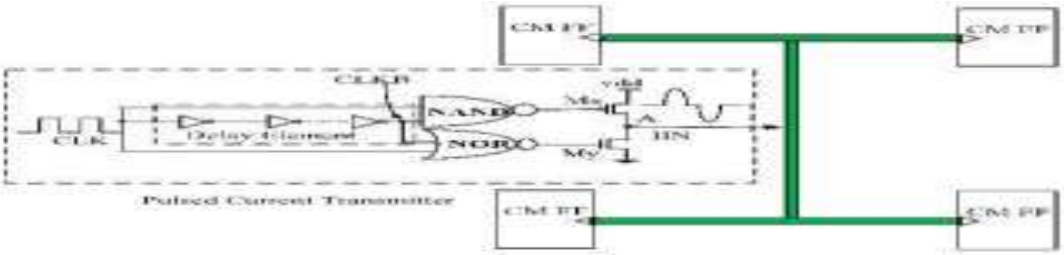

Fig. 1. Previously reported CM clocking scheme saves significant CDN power and exhibits high robustness due to noise and variation, however, only limited to work at symmetric clock networks.

There are two circuits needed to implement the standard point-to-point CM scheme: a transmitter (TX) and a receiver (Rx). The Rx circuit accomplishes the inverse of what the Tx circuit does, which is to convert a VM signal to a CM signal. These point-to-point studies have been done before. off-chip and on-chip communication networks. Nevertheless, they have not taken into account point-to-many dispersion, which clock networks need. An improved point-to-many clocking technique provided considerable power and performance gains over classic point-to-point clock schemes as illustrated in Fig. 1. In order to make this system more efficient, it employs a low-power CM flip-flop (CM FF) and efficient CM clocking. Rather of using a NAND–NOR Tx, the CM-FF-based device employed a current pulse generated from a single source VM signal. The Tx created and transmitted the current pulse, which was synced to the rising edge of the input VM clock signal at the Tx. This made it possible for the Rx circuit in CM FFs to operate on an edge-triggered basis. In comparison to other VM clocking techniques, this one not only used less power, but it also proved to be far more noise resistant. There was, however, no demonstration of the CM pulsed technique in an asymmetric clock network.. Due to CM design flaws, this requires a different approach.

CURRENT-MODECLOCKINGISSUES

This is the minimum current required to charge up a CM FF input enough to let it to

hold an additional value. At about [(Vdd)/2], the clock tree maintains a stable state, and the current pulse comes very immediately. As a result, unlike VM clocks, delay-induced skew is not a serious concern. To avoid CM FF timing distortion, however, each FF requires an identical amount of current. Due of the length of time, this is the most difficult part. **andpeak,andhencetotalcharge,ofthecurrentpulsemustbewithinbounds.**

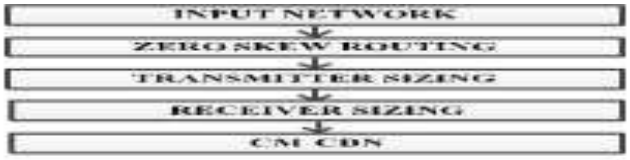

Fig. 3. Flowchart of the proposed CMCS scheme uses a zero-skew unbuffered clock routing along with stages to set the bias voltage with Tx sizing and Rx sizing to minimize skew and maintain correct functionality.

The FF input impedance changes dependingTx bias point, which basically implies the CM FF adjusts input impedance during a typical clock pulse if there are modest bias variations during an average clock pulse. Branching points determine the amount of current that can be directed at each branch, which in turn affects the amount of current that can be directed at downstream FFs. As a result of this difficulty, earlier CM clocking was limited to symmetric H-tree configurations only. An incorrect trip current might cause the CLKP voltage pulse (CM FF voltage pulse) to be skewed in the time domain, which results in an inaccurate clock. This error may be corrected.

increasequicklyinlargerasymmetricnetworkswith largevariationincurrentatthesinks.Intheworstcase,aCMFFmaynot respond if the trip current is insufficient,whichcanresultinafunctionalfailure .Hence, it is desirable touse an automatedsynthesis tool not only for the automation oftheroutingandimpedancebalancingbutalso to ensure the electrical correctness andfunctionality.

VM clock synthesis techniques typically useElmoredelaymodelsforinitialclockroutingandtheninsertandbalancebuffersto constrain the network's slew rates. SincetheElmoredelaymodelisbasedonthecharging/dischargingofacapacitancethrougharesistance,itisnotsuitableforCMsynthesis,becauseCM clockingmaintains a steady-state voltage in the entireclocknetwork.Elmoredelay-basedclockroutingbalancesdelaysinclockbranches,whichisnotthesameasbalancingimpedances.However,itisareasonablestarting point and can be compensated for byappropriatelysizingtheTxandtheRxcircuitryinthe CMFF.

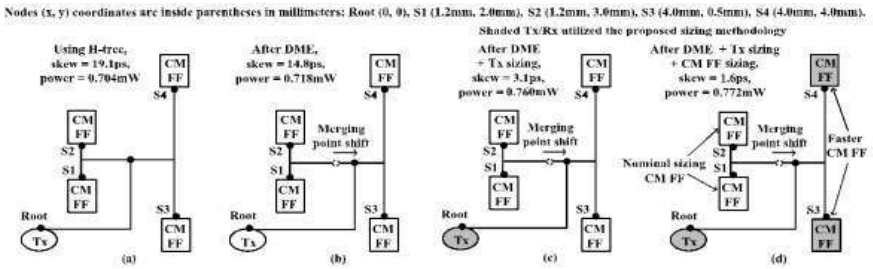

Fig. 2. Both symmetric and DME VM synthesis techniques introduce large skews (19.1 and 14.8 ps, respectively) when directly applied to asymmetric CM clock distributions, however, DME with Tx or combined Tx/Rx sizing methodology can improve the clock skew to 3.1 and 1.6 ps, respectively, with almost equal power consumption in each case.

A computerized approach to calculating Tx and CM FF Rx sizes is presented in our study. This technique is a radical departure from the current impedance balancing VM methods, which rely on clustering and load balancing.balancingwasachievedusingwireand /orbuffersizing.Eventimingmodel-independentschemesutilizedextrawiresanddummysinkstobalancethenetwork,butthesescheme sareonlysuitableforbuffered VM clocking, since the CM FF alsohave varying inputimpedance.

PROPOSEDCURRENT-MODECLOCKSYNTHESIS

An effective CM clocking method relies heavily on the durability and general performance of the Tx/CM FF circuits and their transistor sizes. The upside, on the other hand, is a significant reduction in power consumption with comparable skews as compared to current buffered VM clocking methods. DME tree construction is presented in Figure 3 as the basis for the proposed CM clock synthesis (CMCS) technique. The impedance matching will not be perfect, but this is an excellent starting place. Tx sizing is done to obtain the correct bias voltage for the network, and then Rx sizing in the CM FFs is used to improve the skew.

A.CMPulsedCurrentTransmitterSizing

In the proposed CM clock networks, the CM TX is driven at the root of the network. When used with the CM TX, which produces a push-pull current, the devices are sized to keep the network's bias voltage at a constant level. The TX may have numerous exponentially tapering stages of buffers driving it, which will be included in our subsequent findings. Our CM pulsed current TX sizing technique is described in full in In order to establish a link between TX sizing and the network's total capacitive admittance (YT), we conducted a number of simulations on a variety of network sizes and topologies. Figure 4 depicts the findings of these investigations. The link between YT and TX size is very linear. We compute the network's total impedance in order to establish a relationship between the overall driving load and the TX's size. When it comes to parallel networks, admittance, which is the opposite of impedance, is used. A network's total admittance is inversely proportional to its current, as seen in Figure 4. A CDN's total admission is determined by taking into account the FF and RC networks as a whole.

Empirically, the TX sizing is convex, so weused steepest descent search to find the

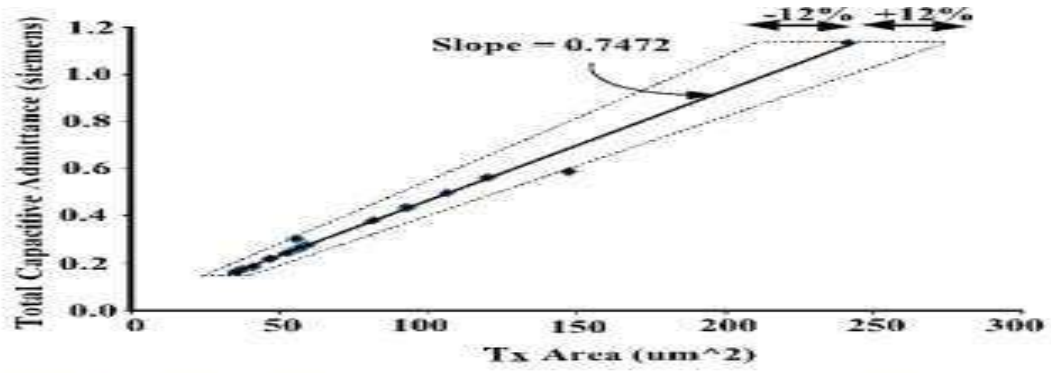

Fig. 4. Ideal CM Tx sizing varies linearly with the total capacitive admittance of the clock network, which allows linear fitting for a starting Tx size.

bestsize.TheTXsizingalgorithmfirstcalculates YT of the network (Line 4) in thetotalAdmittance(Tree)methodwhichapplies.Then,itdeterminestheinitialTXsizing (Tinit) of the network (Line 5) usingsizeTransmitter(YT).Itrunsatransientsimulation(simulateTransient())anduses

calculate Skew () to measure the initial skew(Sinit). Tbest and Sbest are set to the initialvalues(TinitandSinit),respectively.TheTinit value is also stored in two temporaryvariables(TnewUpandTnewDown).

Receiver/CMFFSizingMethodology

We use a limited selection of predesigned CM FF library cells with various input impedances to help in skew optimization. Figure 5 shows a diode-connected inverter circuit coupled to an input reference voltage generator (Mr1–Mr2) whose resistance (AR) may be varied to alter the input impedance. However, in order to accurately measure the CM FF's trip current, both the input reference voltage generator and the local reference-voltage generator (Mr3–Mr4) must have the same AR. As a result, both voltage generators' ARs are changed at the same time. In the current comparator, this results in a voltage fluctuation at the input, which may change

the bias point. Also, the delay between CLK-CLKP is affected by changes in bias voltage. An imbalanced tree is prevented from entering the system by using a technique that selects cells from a CM FF library to balance the root. It's possible to balance any skew by using these cells since they have distinct admittances and hence varying internal CLK-CLKP delays. Starting with a CLK-CLKP delay FF with a median CLK-CLKP impedance, we replace them with lower or higher impedance (slower or faster) variations.

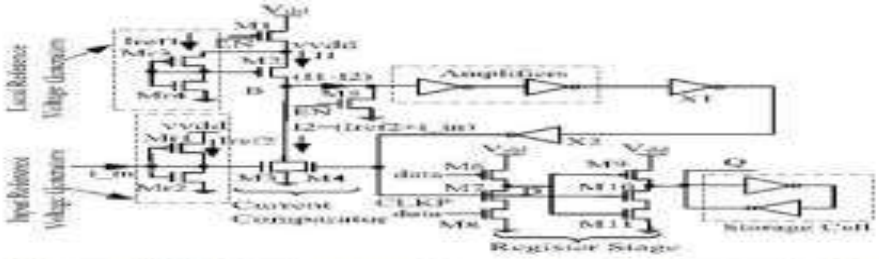

Fig. 3. Sizing of CM FF reference-voltage generators changes the FF internal CLK-CLKP time resulting in faster or slower FF with no impact on FF timing constraint [7].

Any SB window's greatest cluster of "good" sinks is identified by this function's f method. Counting the amount of delays d j inside an SB from sink I with delay di is accomplished by iterating through a list of sinks ordered by delay (Din). If the number of sinks is high enough, the critical sink set C will have the smallest number of CM FFs. As a result, these "critical" sinks fall beyond the range in which the best speed may be achieved.Once the SB is attained, the sizing method suggested in this paper converges to the minimal skew. According to the previous step, the TX size was established, and the CM FF was designed to satisfy the SB for the set TX size. Unlike the Rxs, the TX is not sized after them. As a result, sizing the TX is no longer necessary. Additionally, the CM FFs are lightning-fast, and Algorithm assures thateach FF by properly sizing the CM pulsedcurrentTX.FFmetstabilityisusuallydueto theinputarrivingduringaclocktransition.OurCM FFstillhassetupandholds times like VM FFs to avoid any suchproblems.

SIMULATIONRESULTS

WeimplementedtheproposedCMCSschemeinC++andPython.SimulationswererunonanIntelCorei5-3570IvyBridge3.4-GHzquad-coreprocessor.Wevalidatetheproposedmethodologyusing45-nmISPD2009and2010industrialBenchmarks.ISPD2009benchmarksarederived from real IBM application specificintegratedcircuitsdesigns.Thesebench mark circuits are distributed in 50.4–275.6-mm2areaandconsistsof81–623evenly/unevenly distributed sinks with equalorunequalsinkcapacitances.ISPD2010benchmarks are derived from real IBM andIntelMicroprocessordesigns.The2010benchmarkcircuitsaredistributedin1.4–91.0-mm2 area and consists of 981–2249 nouniformlydistributedsinkswithdifferentloadings.Ourdesignswereoptimizedfor1Vsupplyvoltageandclockfrequenciesrangefrom1–3GHz.Traditionally,5%–10%oftheclockperiodisallocatedforclock skew, so we used a clock SB of 70 psfor1-GHzclockfrequency.Traditionally,worst case slew rate is defined as 10% of theclock period. For the proposed CM clockingschemes,weused10%SB.Itisworthmentioning that at steady state the CM clocktree remain roughly around [(Vdd)/2], hencewe only consideredworstcaseslewrateatthe CLKP signal of CM FF. The CM Tx andRx/FFweredesignedusingtheFreePDK 45-nmCMOS technology. We used HSPICEtomeasurepowerandperformanceforall results.

In a CM scheme, most of the power is staticpower consumed by the CM FFsand therearenoCDNbuffers,soitishighlyinsensitivetofrequency.Becauseofthis,CMclockingsavesquadraticallymorepowerathigherfrequencies,whichisextremelyimportantinmultigigahertzdesigns.Fig.9showstheevidenceoftheproposedCMCSmethodologyefficiencycomparedwithVMbufferedschemeathigherfrequenciesusingISPD200

9benchmarkcircuits4r3.Inparticular,thepower saving of CM methodology increasesfrom 68% (at 1 GHz) to 84% (at 3 GHz)comparedwithVMscheme.

Skew Comparison: The proposed algorithmreduces skew by Tx and CM FF sizing whileensuringcorrectfunctionality.TheCMCSm ethodology resulted in proper functionalityin all of the asymmetric networks. The skewslightlydegradedonaverageinboththe200 9and2010benchmarks,buttheskewresults were better on some benchmarks, asshown in psaverageskewdifferencecomparedwith VMschemeforISPD2009andISPD2010testbenches,respectively. Tables I and II. These skew levelsare well within tolerablelimits of 5%–10%of the clock period and are, therefore, not aconcernespeciallyconsideringthelargepowerc onsumptionsavings.Inaddition,eachschemeus esadifferentmethodologyandtheresponsetoop timizationisnotpredictable. This is common with any sort ofheuristic optimization algorithm, which mayend up in a solution that is closer or furtherfromoptimal.However,overall,theprop osed CM scheme has only 3.3- and 3.9-

RESULTS

ProposeddesigninTannerEDA

Simulation results

CONCLUSION

First-ever CMCS approach has been provided. Here's how it's done:It was necessary to employ TX and Rx sizes in order to assure optimal operation and minimize skew. As compared to industry norms, the suggested technique conserved 39–84 percent average electricity. It used up to 26% less semiconductor space and 2.4x9.1x less run time than buffered virtual machine networks.

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