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Multiple Level and Section Interleave LLC Converter With More Advantageous Strength Processing Capabilities And Herbal Contemporary Day. Sharing

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Abstract An interleaved flying-capacitor LLC converter architecture with high output current applications is introduced in this study. the number one facet's switches are less stressed by a single capacitance in the new converter compared to a traditional-section LLC converter. mechanically balancing the contemporary distribution of phases, and enhancing the strength processing abilities. The advantages of LLC converters, such as zero-voltage switching on the first side's MOSFETs, 0-cutting-edge switching on the second side's power devices, small switching frequency range, and simple architecture, are maintained. An explanation of the converter's basic functioning and analysis is provided, as are the converter's major features and the influence of subpar components on contemporary sharing behaviour In order to demonstrate the enticing features of the new converter, an experimental 600W, 400V-to-12V prototype is utilised to demonstrate exceptional current sharing, easy implementation and excessive performance of up to 97.3 percent.
Resonant power conversion, current sharing, and LLC Converters are all used as index words for this paper..

I. INTRODUCTION

To meet the demands of today's power converters, they must produce greater power and maintain high efficiency across a broad variety of loads. When it comes to front-end DC-DC conversion, the zero-voltage switching (ZVS) for primary side MOSFETs and the zero-current switching (ZCS) for secondary side power devices are two advantages of LLC resonant converter architecture [1]-[5]. Because the transformer leakage inductance is used as the resonant inductor, this device has a small switching frequency range, a quick transient response, and a cheap cost. Switching mode power supplies (SMPSs) are under increasing pressure to become more efficient and power dense, which is why the architecture has found widespread use in devices like flat-panel TVs, 80+ ATX, and small form factor PCs.Multiple converters, or multiphase operation, is an excellent option for distributing the current stress in high-power applications, and it has been extensively studied for both PWM [6]-[10], and resonant converters, [11]-[13]. Multi-phase operation of LLC converters has been discovered to present implementation issues. challenges that are typically related to the load current sharing between the converter's phases [11]-[24]. Current sharing is required to increase the power processing capability, maintain high efficiency and improve the reliability since the thermal stress is better distributed. Therefore, current sharing is considered mandatory in multi-phase LLC converters operation. Due to differences in the resonant networks, an imbalanced load sharing across converter phases is the norm. Mismatches in the resonant tank components affect the current distribution across phases when phases are interleaved because the operation depends on the equivalent switching frequency of the various phases [13].

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This is due to the fact that only one phase is operating at the appropriate frequency. Resonant components values' tolerances may have a considerable impact on current sharing, and one phase can supply most of the load current while other phases deliver a much lower part [19]. [12]-[24] have offered a variety of ways to share the present state. In order to match the values of the resonant tank components, active or passive solutions are used. To regulate the resonant tank capacitance (13), inductance (14), the switching frequency (16), or the phase shift between the phases in a three-phase structure (17), extra circuitry is included in the active solutions. Complicated challenges with management and execution plague many systems, as do the large component count and hefty price tags. Using a common capacitor [18] or common inductor [19], [20] for impedance matching, passive methods may be used for phase matching. Series-input linked capacitors [22, 23] are another passive option that provides effective current sharing.Multi-level operation has been researched to increase LLC resonant converters' power processing performance [25]. Allows for lower voltage rated MOSFETs with a lower RDS(on) per silicon area to be used on the main side's power devices. Conduction losses in a particular region may be reduced while switching losses caused by ZVS are kept to a minimum by using MOSFETs rated at a lower voltage. As an additional benefit of multi-level operation, less energy is stored in the MOSFETs' parasitic capacitances. This reduces the amount of time it takes to attain ZVS and so increases the efficiency of the converter.We want to develop a two-phase interleaved flying-capacitor LLC (TIFLLC) resonant converter topology that combines multiple phases and several levels of operation. This is our goal. With the flying-capacitor in Fig. 1, the main side's MOSFETs are less stressed, the two phases are more evenly distributed, and the power processing characteristics are improved. The TIFLLC converter topology has the benefit of

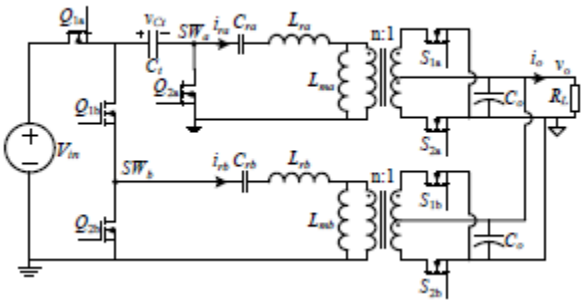

Fig. ***1. Two-phase interleaved flying-capacitor LLC (TIFLLC) converter topology.***

it preserves the benefits of conventional LLC converters such as soft-switching on all power devices, wide load range, narrow switching frequency range as well as excels with high efficiency. These advantages make the topology an attractive candidate for high output current applications. The rest of the paper is organized as follows: Section II presents the TIFLLC converter topology principle of operation and provides typical key waveforms of the new converter. Design considerations and details regarding the flying-capacitor are provided in Section III. Next, the current sharing and enhanced power processing characteristics are described and analyzed in Section IV. Implementation of the TIFLLC prototype and experimental results are provided in Section V. Section VI concludes the paper.

II. PRINCIPLE OF OPERATION

The TIFLLC converter, shown in Fig. 1, combines the benefits of a switched-capacitor circuit and a series-resonant LLC converter. This topology adds a single capacitor *Ct* to the component count of a conventional two-phase LLC converter, depicted in Fig. 2. The converter's configuration and waveforms resemble the ones of the two-phase interleaved LLC converter, with the benefits of lower voltage stress transistors.

The operation of the TIFLLC converter is similar to the one of a conventional two-phase interleaved LLC converter with 1800 phase delay, i.e., when the switching node (*SWa* or *SWb*) of one phase is high, then the switching node of the other phase is low. However, it should be noted that while in conventional two-phase interleaved LLC converter the phase delay between the phases can be arbitrarily selected (typically selected to be 900 to reduce the output voltage ripple) the 1800 phase delay in the TIFLLC converter cannot be changed and therefore it doesn't contribute to output voltage ripple reduction. Therefore, two switching states are recognized as shown in Fig. 3 with the corresponding waveforms

(obtained by a PSIM simulation) shown in Fig. 4: State I: phase *a* is on and phase *b* is off; State II: phase *a* is off and phase *b* is on.

In state I, depicted in Fig. 3(a), switches *Q*1a and *Q*2b are on, the input voltage connects to phase *a* through the flying-capacitor *Ct* and the applied voltage on its resonant tank is *V*in- *VCt*, while the resonant tank of phase *b* connects to ground via *Q*2b. At the secondary side, switches *S*2a and *S*1b are on for synchronous rectification operation. State II is shown in Fig. 3(b). Here, switches *Q*1b and *Q*2a are on and the flying-capacitor acts as the source for phase *b*, imposing a voltage of *VCt* on its resonant tank, while the resonant tank of phase *a* connects to ground; switches *S*1a and *S*2b are on for synchronous rectification of the output current. As in conventional LLC

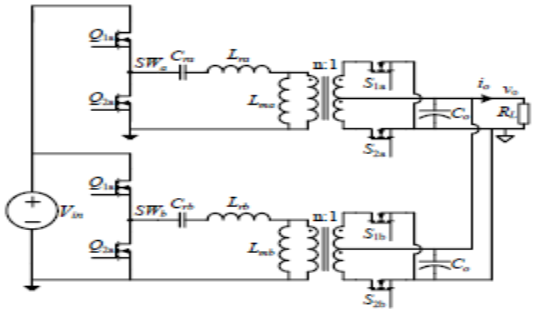

Fig. 2. Conventional two-phase LLC converter.

resonant converters, dead-time between the two switching states is added to facilitate ZVS for the primary side's MOSFETs, and ZCS is obtained for the secondary side's power devices. It should be noted that *Ct* is designed to be significantly larger than the resonant capacitors and therefore it acts as a voltage source that has minor effect or none on the resonant behavior of the converter's phases. Further design details regarding the flying-capacitor are provided in Section III.

As can be observed from Fig. 3 and Fig. 4, the operation of the TIFLLC converter topology resembles a two-phase interleaved LLC converter with two input voltages for each phase that sum to *V*in. As will be detailed in the next section, these input voltages adapt their value based on the voltage gain per phase and as a result, high immunity is achieved to mismatches between the phases' resonant components. In addition, the use of a flying-capacitor naturally equalizes the current distribution the current between the phases, which in turn, enhances the power processing characteristics of the converter.

III. ANALYSIS OF PRIMARY CHARACTERISTICS FOR THE TIFLLC CONVERTER TOPOLOGY

The flying-capacitor used in the TIFLLC converter introduces several interesting characteristics. The applied voltage on the switching nodes *SWa* and *SWb* is half of the input voltage which lowers the voltage stress on three out of the four primary side's MOSFETs by half. It also allows for lenient conditions to achieve ZVS on all the primary side's MOSFETs, since the voltage swing on these transistors during the commutation period is only half the input voltage. Moreover, the applied voltage on the resonant tank is also lowered by half and allows a design of a resonant network with lower impedance, i.e. lower inductance for the same switching frequency. Another very important property that will be detailed in the next section is the charge-balance on the flying-capacitor that provides current distribution between the converter's phases.

The voltage of the flying-capacitor *vCt* is assumed constant *VCt* for a duration of a switching cycle due to its low voltage ripple. The flying-capacitor's voltage ripple Δ*vCt* depends primarily on the load current and it is designed to be small, i.e. no more than 5% of the nominal value of *VCt* that typically equals *V*in/2. This selection of a sufficiently high flying-capacitor value also guarantees that the tanks' resonant frequency is not affected by this capacitor. The expression for

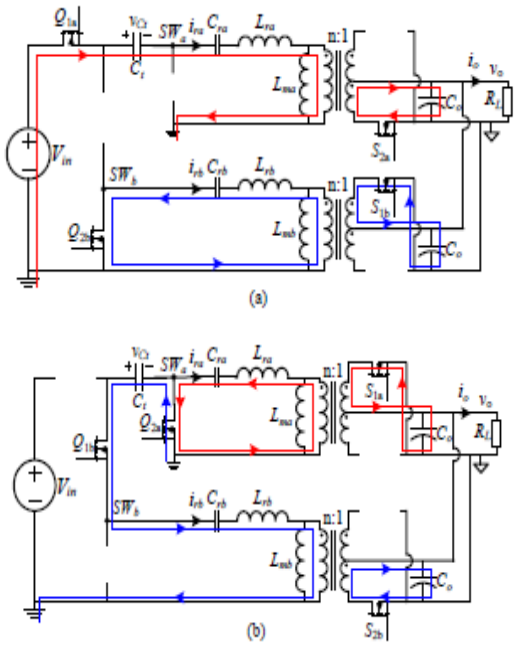

Fig. 3. Current paths in the TIFLLC converter: (a) State I: phase a is on and phase b is off, (b) State II: phase a is off and phase b is on.

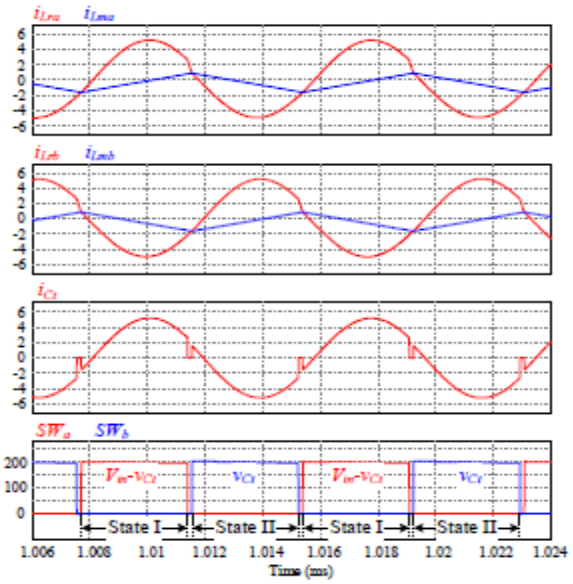

Fig. 4. Typical waveforms of the TIFLLC converter.

Δ*vCt* is calculated by the charge being transferred in each state, and can be expressed as

$$\Delta v_{Ct} = \frac{I_{out}}{4nf_s C_t}, \qquad (1)$$

where *Iout* is the load current, *fs* is the switching frequency and *n* is the transformer's turns ratio.
The DC voltage of the flying-capacitor in the ideal case, i.e. the case of identical resonant components for both phases, equals *Vin*/2. For any other case, there may be a drift of *VCt* which is a result of the gain difference between the phases. Under first harmonic approximation (FHA) the normalized voltage gains *Ga* and *Gb* (for phases *a* and *b*, respectively) are

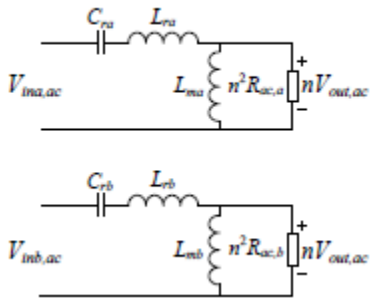

Fig. 5. Equivalent model of the TIFLLC converter using first harmonic approximation.

expressed as (obtained by the equivalent circuit shown in Fig. 5):

$$G_a(f_s) = \frac{nV_{out,ac}}{V_{ina,ac}} = \frac{1}{\left(1+\frac{L_{ra}}{L_{ma}}-\frac{L_{ra}}{L_{ma}}\frac{1}{f_{na}^2}\right)+j\frac{\sqrt{L_{ra}/C_{ra}}}{n^2R_{ac,a}}\left(f_{na}-\frac{1}{f_{na}}\right)} \qquad (2)$$

$$G_b(f_s) = \frac{nV_{out,ac}}{V_{inb,ac}} = \frac{1}{\left(1+\frac{L_{rb}}{L_{mb}}-\frac{L_{rb}}{L_{mb}}\frac{1}{f_{nb}^2}\right)+j\frac{\sqrt{L_{rb}/C_{rb}}}{n^2R_{ac,b}}\left(f_{nb}-\frac{1}{f_{nb}}\right)} \qquad (3)$$

where *Vina,ac* and *Vinb,ac* are the ac input voltages of the phases *a* and *b*, respectively, given by:

$$V_{ina,ac} = \frac{V_{in}-V_{Ct}}{2},\ V_{inb,ac} = \frac{V_{Ct}}{2}, \qquad (4)$$

and *fna*, *fnb* are the normalized switching frequencies of phases *a* and *b*, defined as:

$$f_{na} = \frac{f_s}{f_{ra}} = \frac{f_s}{1/2\pi\sqrt{L_{ra}C_{ra}}},\quad f_{nb} = \frac{f_s}{f_{rb}} = \frac{f_s}{1/2\pi\sqrt{L_{rb}C_{rb}}} \qquad (5)$$

Using (2)-(4) and after some manipulations, the flying-capacitor voltage can be extracted and expressed as:

$$V_{Ct}(f_s) = \frac{V_{in}}{1+\frac{|G_b(f_s)|}{|G_a(f_s)|}}. \qquad (6)$$

This implies that in case that the voltage gains of the phases are not equal, e.g. due to components' tolerances, the voltage deviates from the *Vin*/2 value and also depends on the switching frequency. Fig. 6 shows the variance in flying-capacitor voltage as a result of components' difference between the phases as a function of the normalized switching frequency, where in each case a different component has been changed and the case study parameters are detailed in Table I. It can observed that for higher output power the voltage deviation from 200V is smaller compared to lower output power. It can also be observed that

the overall deviation, even for the lower power case, is relatively small for the switching frequency's area of interest (marked with arrow on Fig. 6) where ZVS on the primary-side's MOSFETs is achieved and the voltage gain is not highly dependent on the load, i.e. above 0.6*fr*. Lower frequencies than 0.6*fr* may enter the capacitive region for some load conditions which may result in high switching losses and

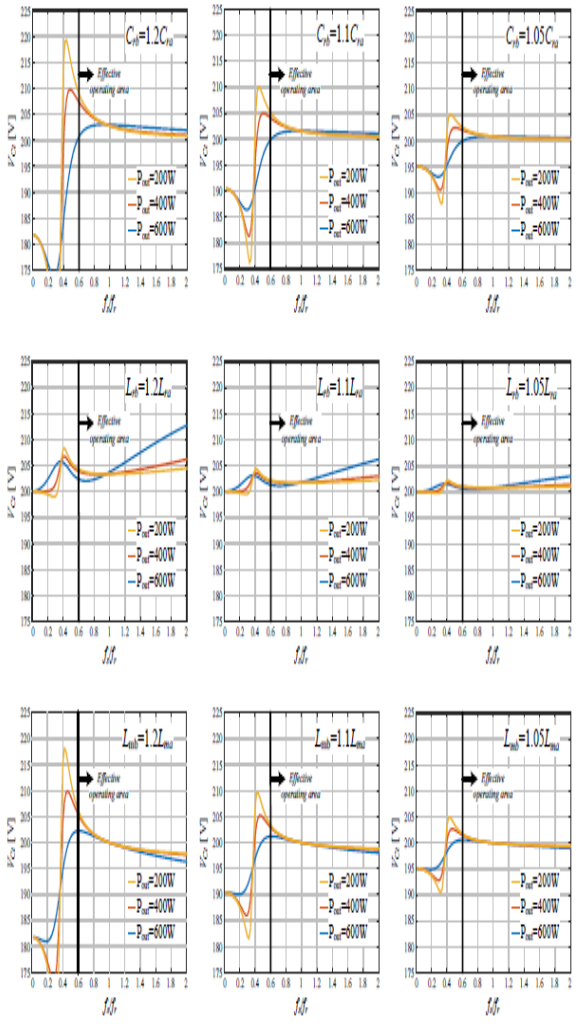

Fig. 6. Flying-capacitor voltage as a function of the switching frequency for phases with different resonant tank's parameters.

TABLE I – CASE STUDY PARAMETERS VALUES

Component	*Value / Type*
Input voltage V_{in}	400 V
Output voltage V_o	12 V
Transformers' turns ratio n	8
Phase a resonant frequency f_r	~150 KHz
Phase a resonant capacitor C_{ra}	44 nF
Phase a resonant inductor L_{ra}	25 µH
Phase a magnetizing inductor L_{ma}	150 µH

Reduced efficiency. It should be noted that the value of 0.6*fr* is only relevant for the presented case study and it different for every converter's design. Fig. 7 presents the variance in the flying-capacitor voltage for the worst case scenario where all the resonant tank's components of one phase have 20% variation compared to the other phase. As can be observed, even for such extreme conditions the voltage deviation is small and therefore has minor effect on the converter's operation.

As in any capacitor based multi-level converter, there is an issue during start-up operation when the flying-capacitor is discharged of voltage stress on some of the MOSFETs. A possible solution to solve this problem and avoid any high inrush current to charge the flying-capacitor has been presented in [26], where an additional switch and a resistor have been connected in parallel with a low voltage MOSFET to limit any inrush current during start-up. Since the required capacitance

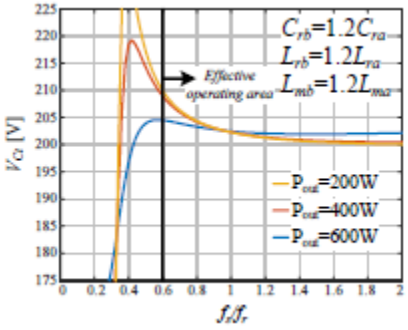

Fig. 7. Flying-capacitor voltage as a function of the switching frequency for worst-case resonant tank component's variation between the phases.

of the flying-capacitor in the TIFLLC converter is relatively small, its charging time can be much shorter than an overall start-up procedure that includes soft-start.

IV. CURRENT SHARING UNDER PARAMETER VARIATIONS

Current sharing of multi-phase LLC converters has been widely investigated in [12]-[24]. In the TIFLLC converter topology, the charge-balance of the flying-

capacitor assists in passive current sharing between the phases. Two MOSFETs

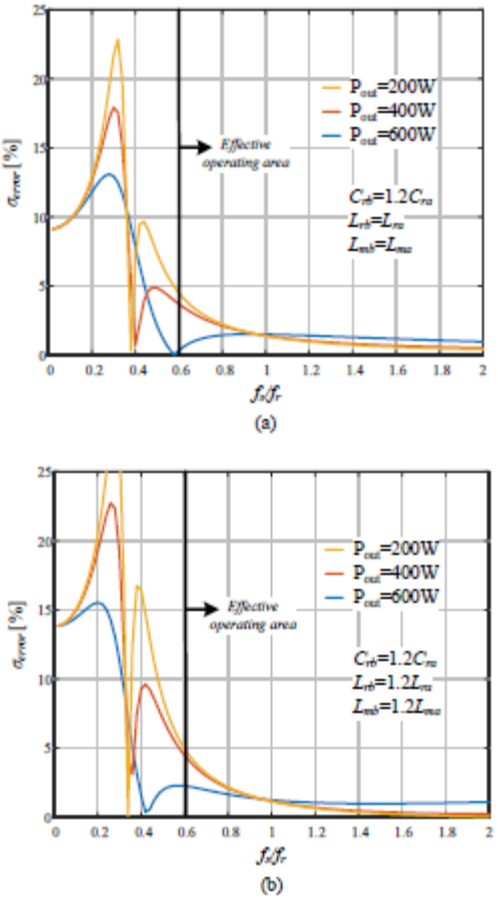

Fig. 8. Current error between the phases as a function of the switching frequency for: (a) *Crb*=1.2*Cra*, (b) worst case component's mismatch: *Crb*=1.2*Cra*, *Lrb*=1.2*Lra*, *Lmb*=1.2*Lma*.

conduct the current of the flying-capacitor: these are *Q*1a during state I and *Q*1b during state II, i.e.

$$i_{Ci} = \begin{cases} i_{Q1a} & @state\ I \\ -i_{Q1b} & @state\ II \end{cases} . \qquad (7)$$

Since charge-balance on this capacitor exists, the average current through it must be zero, and the average currents through these two MOSFETs in every switching cycle are equal, i.e.

$$\langle i_{Q1a} \rangle = \langle i_{Q1b} \rangle . \qquad (8)$$

Neglecting power loss in the system and assuming that the efficiency is high, the following holds

$$\begin{aligned} P_{in,a} &= P_{out,a} \\ P_{in,b} &= P_{out,b} \end{aligned} , \qquad (9)$$

where *Pin* and *Pout* are the average input and output powers of each phase. The equality of (9) can be rewritten as

$$\begin{aligned} P_{in,a} &= \langle v_{in,a} \rangle \langle i_{in,a} \rangle = \frac{V_{in} - V_{Ci}}{2} \langle i_{Q1a} \rangle = I_{out,a}^2 R_{ac,a} = V_{out} I_{out,a} \\ P_{in,b} &= \langle v_{in,b} \rangle \langle i_{in,b} \rangle = \frac{V_{Ci}}{2} \langle i_{Q1b} \rangle = I_{out,b}^2 R_{ac,b} = V_{out} I_{out,b} \end{aligned} \qquad (10)$$

where *Iout,a* and *Iout,b* are the average output currents of the phases. From (8)-(10) it can be derived that the ratio between the two phases' output currents equals the ratio between the input voltages of the two phases, i.e.:

$$\frac{I_{out,a}}{I_{out,b}} = \frac{V_{in,a}}{V_{in,b}} = \frac{V_{in} - V_{Ci}}{V_{Ci}} . \qquad (11)$$

The expression in (11) provides an insight to the current sharing mechanism that is achieved with the usage of the flying-capacitor. The voltage *VCt*, as opposed to *Vin*, can dynamically change and as a result both *Vin,a* and *Vin,b* would vary accordingly. In the case that both the input and output voltages are common for the two phases, a mismatch of the resonant components results in voltage gains *Ga* and *Gb* that differ from the effective input-to-output ratio. The operation of the flying-capacitor automatically corrects the effective phase's input voltage (and as a result the input-to-output ratio) to comply with the variation in the voltage gain. It should be noted that this balancing action of the input voltages of the phases exceeds beyond the simplistic property of components variations for other parameters of the system such as the turn ratios of the phases' transformers.

Using the expression given in (6) and after some manipulations, the ratio between the phases' output currents can be expressed as

$$\frac{I_{out,a}}{I_{out,b}} = \frac{G_b}{G_a} , \qquad (12)$$

where *Ga* and *Gb* are given in (2) and (3). The current error between the two phases (the ratio between the difference and sum of the output currents, as defined in [19]), can be now expressed as

$$\sigma_{error} = \left| \frac{G_a - G_b}{G_a + G_b} \right|. \qquad (13)$$

Fig. 8 shows the value of (13) as a function of the switching frequency and the output power for a case of a converter with parameters that are as given in Table I, and the variation in the resonant capacitor of phase *b* is by 20% compared to the resonant capacitor of phase *a*, and for the worst case scenario where all the resonant tank' components have 20% variation. It can be observed that for a switching frequency higher than 0.6*fr* the current error is less than 5% for both cases, which is an attractive attribute for passive current sharing even at such an extreme case of components' difference.

The very good current distribution in the TIFLLC converter topology also contributes to enhanced power processing characteristics. The 1800 phase delay between the converter phases provides an interesting feature when *Q*2a is on. During the period of state II *Q*2a has two main purposes, one is applying a low potential path for the resonant current of phase *a*, i.e. zero voltage on the resonant tank. The second is connecting the negative port of the flying-capacitor to ground in order to apply *VCt* on the resonant tank of phase *b*. Therefore, *Q*2a participates in the operation of both phases and during state II it passes resonant currents of the two phases simultaneously. Since at this state the resonant currents are in opposite direction (the current in phase *a* is negative whereas the current in phase *b* is positive), the net current flowing through *Q*2a is zero, as shown in Fig. 9. The main contribution to the current rms value of *Q*2a is its current during the dead-time, where the current magnitude equals to the resonant current magnitude, which is not zero. This translates into a more relaxed selection of this switch and implies that a higher on-resistance MOSFET with

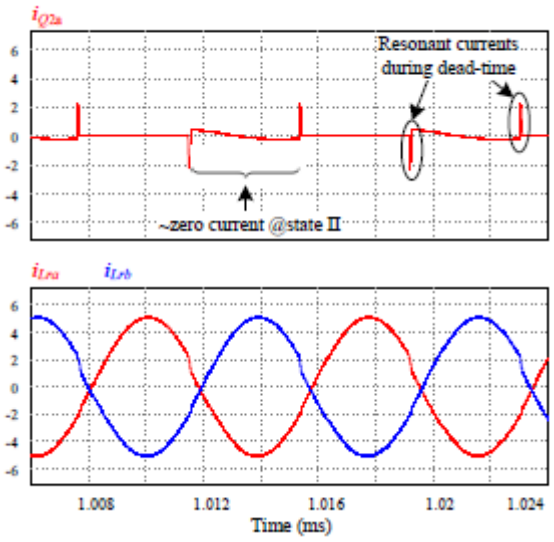

Fig. 9. Zero current characteristic of *Q*2a.

TABLE II – EXPERIMENTAL PROTOTYPE'S PARAMETERS VALUES

Component	*Value / Type*
Input voltage V_{in}	400 V
Output voltage V_o	12 V
Flying capacitor C_r	3 µF
Output capacitance C_{out}	1 mF
Phase *a* transformer's turns ratio n_a	9
Phase *b* transformer's turns ratio n_b	9.3
Phase *a* resonant frequency f_{ra}	~138 KHz
Phase *b* resonant frequency f_{rb}	~130 KHz
Phase *a* resonant capacitor C_{ra}	66 nF ±10%
Phase *b* resonant capacitor C_{rb}	66 nF ±10%
Phase *a* resonant inductor L_{ra}	20 µH
Phase *b* resonant inductor L_{rb}	23 µH
Phase *a* magnetizing inductance L_{ma}	150 µH
Phase *a* magnetizing inductance L_{mb}	155 µH
Primary-side gate drivers	UCC27714

Lower capacitances is sufficient for the tasks required by *Q*2a. This selection does not compromise on the efficiency of the converter, which in fact, improves and benefit from a lower required magnetizing inductance circulating current and gate driving requirements.

V. EXPERIMENTAL RESULTS

To validate the operation of the TIFLLC converter operation, a 600W, 400V-to-12V prototype was built and tested. The transformers of both phases were handmade to create a difference between the resonant components of the phases and their measured leakage and magnetizing inductance are detailed in Table II. In addition, to further create a difference between the

phases' parameters, the turn ratios of the transformers were designed to be not equal. The rest of components values and parameters of the TIFLLC experimental prototype are given in Table II. The converter is digitally controlled using an Altera FPGA [27] using fully digital high performance ADC and DPWM peripherals as detailed in [28] and [29].

The control scheme that was used in this study is described by the simplified block diagram of the TIFLLC controller, depicted in Fig. 10. A window-ADC samples the output voltage and compares it with a reference value *Vref* to create an error signal *ve*[*n*] that is the input of a digital PID compensator.

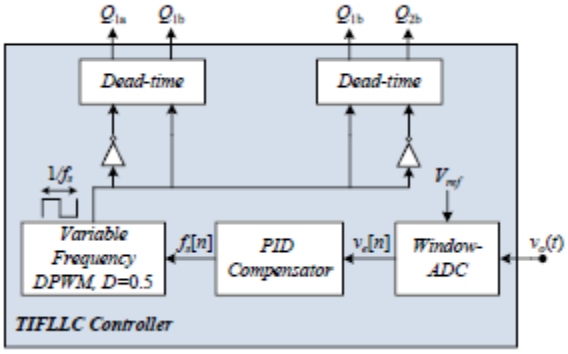

Fig. 10. Simplified block diagram of the TIFLLC controller.

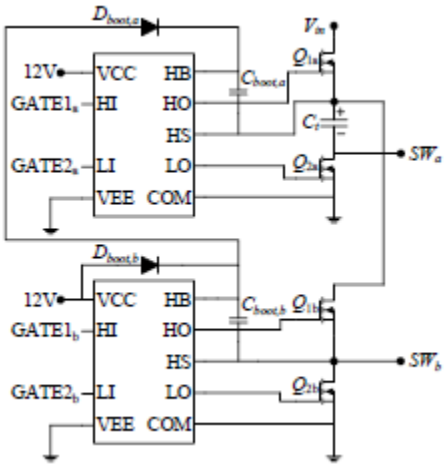

Fig. 11. Gates drivers' realization in the TIFLLC converter.

A PID compensation scheme is used to obtain high loop-gain bandwidth and its output is the frequency of the DPWM *fs*[*n*]. The output of the DPWM is a square wave with frequency *fs* and 0.5 duty-ratio. The square wave is then inverted to create two square waves with 1800 phase delay. At last, two dead-time units are used to create sufficient dead-time between the high and low side gate signals of each phase in order to obtain ZVS on the primary-side's MOSFETs.

A. Implementation of the Primary-Side's MOSFETs Gate Drivers

Although the two phases of the TIFLLC converter are not conventional half bridges, its gate drive circuitry is similar to the gate drive circuitry of a two conventional half bridges transistors assemblies, except for a slight modification in the charging path of the boot capacitor of phase *a*. A simple bootstrap driver cannot be employed for this case since its source (*SWa*) does not meet ground at any time and its bootstrap capacitor would not charge by a drive voltage referenced to ground. To overcome this obstacle, instead of connecting the bootstrap diode of phase *a*'s driver (*Dboot,a*) to a ground referenced drive voltage, it connects the bootstrap capacitor of phase *b*'s driver *Cboot,b*, as shown in Fig. 11. This way when *Q*1b is on, *Cboot,a* is charged by *Cboot,b* through *Dboot,a* in a similar operation to the one of diode-capacitor charge pump. The other MOSFETs driving is simple: *Q*1b and *Q*2b are standard high-side and low-side MOSFETs driven by a dual bootstrap driver configuration and *Q*2a is driven by the low-side driver of the dual bootstrap driver that also drives *Q*1a. The component count of the driving configuration remains the same as the component count of conventional two-phase LLC converter.

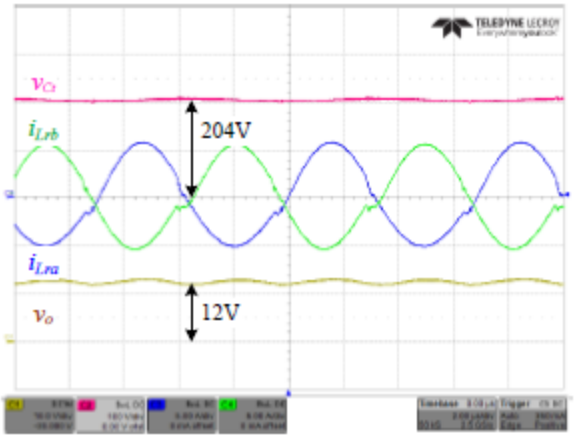

Fig. 12. Experimental waveforms of the TIFLLC converter. C1 – output voltage *vo* (5V/div), C2 – flying-capacitor voltage *vCt* (100V/div), C3 – phase

a primary-side resonant tank current *iLra* (5A/div), C4 – phase *b* primary-side resonant tank current *iLrb* (5A/div). Time scale is 2µs/div.

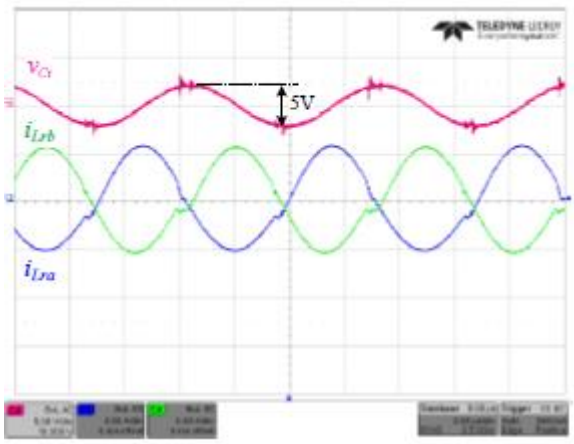

Fig. 13. Experimental waveforms of the TIFLLC converter. C2 – flying-capacitor voltage *vCt* (5V/div, ac coupled), C3 – phase *a* primary-side resonant tank current *iLra* (5A/div), C4 – phase *b* primary-side resonant tank current *iLrb* (5A/div). Time scale is 2µs/div.

B. Experimental Results

Figs. 12 to 14 show the converter's waveforms for output current of 50A (full load). Fig. 12 shows the flying-capacitor voltage, output voltage and the primary-side's currents of the two phases. As can be observed, in spite of the difference between the parameters of the phases, the phases' currents are almost equal with a very small difference between them, with a measured current error of 0.4%. In addition, the flying-capacitor voltage is 204V which is very close to *Vin*/2, as expected by the theoretical analysis from Section III. It should be noted that the output voltage ripple is measured at around 1V, which is the worst case voltage ripple due to operation in full load and a result of relatively small output capacitance used in the experimental prototype. Depicted in Fig. 13 is the voltage ripple of the flying-capacitor Δ*vCt* with a magnitude of around 5V, which is approximately 2.5% of *VCt*. Fig. 14 depicts the switching nodes *SWa* and *SWb*. As can be observed, ZVS of the primary-side's MOSFETs is obtained and the voltage of the switching nodes is around 200V (half of *Vin*) when they are high. Fig. 15 presents the measured current error for the full load range of the converter when the resonant capacitors have equal values (as in Table II) and when one of the resonant capacitors (*Cra*) has been replaced with significantly small capacitor (55nF instead of 66nF) which represents a 20% difference between the phases' capacitors . The results are in

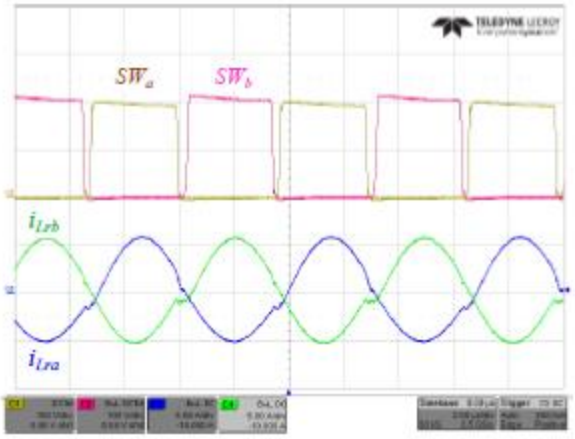

Fig. 14. Experimental waveforms of the TIFLLC converter. C1 – switching node voltage of phase *a* *SWa* (100V/div), C2 – switching node voltage of phase *b* *SWb* (100V/div), C3 – phase *a* primary-side resonant tank current *iLra* (5A/div), C4 – phase *b* primary-side resonant tank current *iLrb* (5A/div). Time scale is 2µs/div.

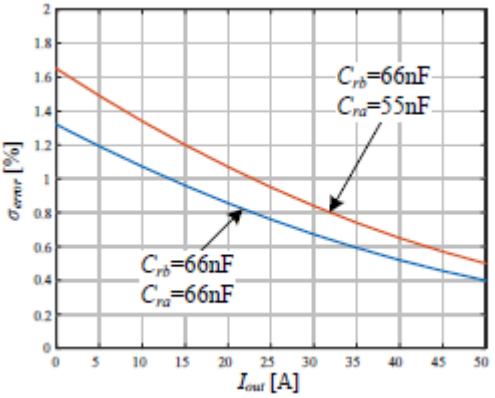

Fig. 15. Measured current error between the phases of the experimental prototype.

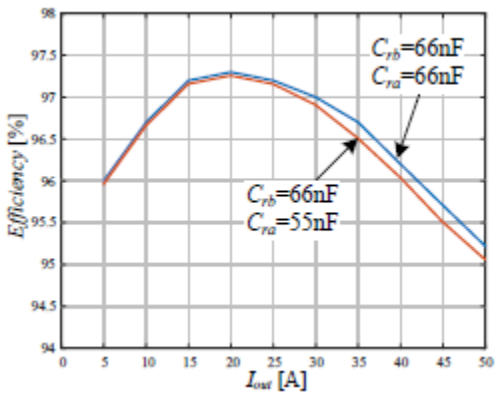

Fig. 16. Efficiency measurements of the experimental prototype.

very good agreement with the analysis from Section IV, verifying the natural current sharing between the phases and the small current error even at large components mismatch. Efficiency measurements of the converter for the two setups are provided in Fig. 16, demonstrating a peak efficiency of 97.3% and above 96% for most of the load range. It can also be observed that the variation of the resonant capacitor has negligibly small effect on efficiency, and its effect is only noticeable at high output currents which is reasonable due to the fact that the conduction losses are dominant and the current sharing error is slightly higher, resulting in one phase that is less efficient than the other.

VI. CONCLUSION

In this work, a novel two-phase interleaved flying capacitor LLC converter architecture was proposed. A flying-capacitor is used to reduce voltage stress on the switches, naturally balance the current distribution across the phases, and boost the power processing capabilities of the two-phase design. While preserving minimal sensitivity to resonant tank parameter mismatches and standard drive circuitry, the converter retains all the advantages of traditional LLC converters. The converter's basic properties and the effect of non-ideal components on current sharing behaviour have been detailed in detail. Using the novel converter as a front-end converter for high output current applications, the practical findings demonstrate promising power processing characteristics and correspond well with the theoretical analysis.

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