ISSN: 2454-9940

# INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

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INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940

www.ijasem.org

Vol 18, Issue.2, 2024

# CASCADED HBRIDGE MULTILEVEL INVERTERS USING A NOVEL SINGLE-CARRIER BASIS PULSE-WIDTH MODULATION TEMPLATE

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## ABSTRACT

Power-conditioning circuit topologies and the associated control/modulation algorithms have seen a noticeable uptick in the field of power electronics in recent times. In a cascaded H-bridge (CHB) multilevel inverter (MLI), the multiplicity of the carrier signals is a requirement for extending sinusoidal pulse width modulation, or SPWM, to multiple output voltage levels. Taking into account medium and high voltage applications that need a large number of CHB MLI output voltage levels. Precise synchronization of these multi-carrier signals is necessary for the CHB MLI system to produce high-quality output waveforms. Real-time digital implementation has challenges in attaining this synchronization due to sampling problems, memory limitations, and computational delays. For CHB MLI, a PWM template is presented in this paper. The suggested control approach modifies a sinusoidal modulating waveform to fit inside a single triangle carrier signal range, generating suitable modulation templates for the CHB inverter. These templates don't need any further control adjustment to be used on CHB inverters of any level. The suggested modulation produced a nearly uniform distribution of switching pulses, an equal distribution of the total real power among the power switches that make up the power switches, and improved output voltage quality. Results from simulations and experiments were reported for a 9-level CHB.

## 1.INTRODUCTION

Power-conditioning circuit topologies and the associated control/modulation algorithms have seen a noticeable uptick in the field of power electronics in recent times. This trend is a direct result of the worldwide effort to find more environmentally acceptable and sustainable sources and applications for electrical power. Inverters and dc-ac converters are essential power electronics components in this scenario. They are used in a number of critical applications, including high-voltage direct-current (HVDC) transmission, Flexible AC Transmission Systems (FACTS), grid integration for renewable energy, energy storage systems, marine propulsion, solar water pumping systems, grinding and rolling mills, compressors, and extruders, to name a few. Power electronics inverters must fulfill certain requirements for this kind of deployment, two of which are high output voltage and a variety of operating output power quality indices.

The most effective gadget for meeting these needs is the multilayer inverter, or MLI. Multilevel inverter power circuit designs have become more common as a result of increased awareness of the inherent potentials of MLIs and their benefits for a variety of industrial applications, as documented in the literature. Upon further examination, these recently developed MLI topologies reveal that they are, in fact, a hybrid or a spin-off of one of the traditional MLI configurations: multilevel inverters with flying capacitors, diode-clamped and capacitor-clamped (CHB). Due to the inherent operating imbalance in the voltages of the constituent capacitor banks, the commonly utilized basic MLI configurations—aside from the CHB MLI—have only been able to synthesize 3-level output voltages.

These three-level designs are now commercially accessible and have reached industrial maturity. Conversely, depending on the application, the CHB MLI topological characteristic enables the synthesis of viable multilayer output voltages. Therefore, the CHB MLI is often selected for high-voltage/power deployment because to its scalability, adaptability, and overall better power quality.

For controlling the frequency and amplitude of the synthesized output voltage waveform of CHB MLI, the most often used modulation approach is triangular carrier-based sinusoidal pulse width modulation, or SPWM. It uses an inverter phase-leg approach to generate gating signals. This means that every phase of the inverter repeats the same control idea; the phase angle shift is the only modulating parameter that varies. In particular, the control idea compares a basic frequency sinusoidal modulating signal with a high frequency triangular carrier wave, setting the zero-sequence signal to zero. In reality, the application of SPWM to multilevel and/or multiphase systems merely requires a multiplicity of the triangular carrier and sinusoidal modulating signals. It poses no rigorous or sophisticated computing challenges. It is a known fact that the two general variations of the SPWM approach that have been well documented in the literature for CHB MLI are the Phase-shifted (PS) and Level-shifted (LS) pulse width modulations.

Of all these modulation schemes, the LS PWM's in-phase disposition (IPD) variation has the greatest harmonic performance; in contrast, the LS PWM's alternative phase-opposite disposition (APOD) variant's harmonic performance is identical to the PS SPWM scheme's. The PS PWM promises higher modulation performance with regard to even power supply from each of the CHBs and equal distribution of switching pulses across power switches of the comprising cascaded cells. To combine the excellent modulation characteristics of PS PWM and IPD PWM schemes, many methods have been proposed for this combinational notion, as shown.

As previously indicated, a fundamental need for the expansion of SPWM to many output voltage levels per inverter phase-leg is the multiplicity of the triangular carrier signals. Stated differently, every phase-leg of an inverter synthetic output voltage level is associated with a generating triangle carrier. It is unavoidable that this inverter arrangement will need a correspondingly large number of triangular carrier signals in either the conventional LS or PS SPWM scheme for medium and high voltage applications where a significant number of synthesized output voltage levels from CHB MLI are required. Furthermore, accurate synchronization of these multicarrier signals is necessary for the CHB MLI system to provide high-quality output parameter waveforms. Sampling problems, memory limitations, and computational delays make it difficult to achieve this synchronization for real-time digital implementations of SPWM methods and generally have a detrimental impact on the dynamic performance of digitally controlled CHB MLI.

The works done in proposed a modified SPWM scheme, wherein the sinusoidal modulating signal is modified to fit in a single triangular carrier range of 0 to 1, in order to generate multi-level waveforms at the output of multilevel converter, in an attempt to remove the traditional requirement of many carrier waveforms in SPWM.

This modulation system was only used in conjunction with the modular multilevel converter (MMC), a more modern invention. The benefits of this SPWM approach are summarized as follows: it requires only one triangular carrier signal per phase; it completely avoids multi-carrier synchronization issues, making it easier to implement digital controllers; it involves simple mathematical operations, making the system computationally less complex; it performs identically to the existing PS SPWM; and it can be extended to MMC with a large number of sub-modules without additional modifications. By focusing on the adaption of CHB MLI, a modified SPWM scheme was suggested for CHB MLI.

It was shown there that, regardless of the number of cascaded H-bridge units, the in-phase disposition (IPD)SPWM method may be used in the synthesis of multiple output voltage levels in CHB MLI using just one triangular carrier signal. Although the authors did, in fact, present a simplified implementation algorithm for their proposed control approach, it is evident that their modulation scheme still exhibits the undesirable features of IPD SPWM, namely, unequal distribution of switching signals among the power switches that comprise the scheme and unequal distribution of the total inverter output power among the CHB units. Phase-shifted SPWM

outperformed inphase level-shifted SPWM in terms of control due to these modulation characteristic properties MLI CHB. To close this gap, it is thus necessary to include these functionalities into the single carrier SPWM paradigm.

This study provides a single carrier-based PWM template for cascading Hbridge multilevel inverters in order to close this gap. Its operating idea is developed from the in-phase disposition level-shifted SPWM operational theory, whereby the necessary output waveform template for the MLI is generated by modifying the sine modulating waveform to fit inside a single triangle carrier signal range. A straightforward reverse-voltsorting technique efficiently eliminates the evident intrinsic flaw of this in-phase , level-shifted SPWM (non-distribution of switching signals to power switches and uneven output power sharing) from the modulation scheme. By mediating between phase- and level-shifted carrier-based SPWM approaches, the suggested control strategy effectively creates a hybrid modulation scheme that inherits the best aspects of each of these modulation systems. Results from simulations and experiments are presented for a three-phase, seven-level CHB inverter.

## 2.BASICS OF H BRIDGE INVERTER

H-bridge Voltage Source Inverter is shown in Fig. 1. Four primary switches and four freewheeling diodes make up each H bridge inverter circuit. Depending on the switching state of the switches, the output voltage may be either positive or negative polarity, or zero volts.

The minimum voltage level for a multilayer inverter that uses a cascaded inverter is three levels CHB. It takes a single full-bridge inverter unit to produce a three-level waveform. A full-bridge inverter is sometimes referred to as an H-bridge cell, as seen in Figure 1. Three output voltage levels, +V, -V, and 0 may be retrieved for the voltages across A and B based on the four-switching combinations pattern.

Switches S1 and S4 are closed simultaneously during inverter operation, as seen in Fig. 1, to provide VAB a positive voltage and a current route for Io. In order to provide VAB a negative voltage and the route for Io illustrated in Figure 2, switches S2 and S4 are switched on. The electricity flows via the freewheeling diodes when every switch is off. Two switching patterns may be used to achieve zero level in the event of zero level, for instance: (1) S1 S2 on, S3 S4 off S3 S4 on, S1 S2 off. Any of them may be used to reach the zero level.

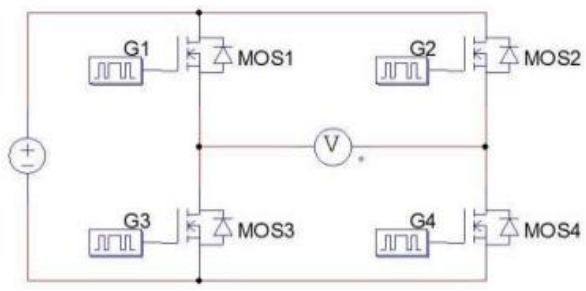



Fig:2.1 Diagram for basic H-Bridge structure

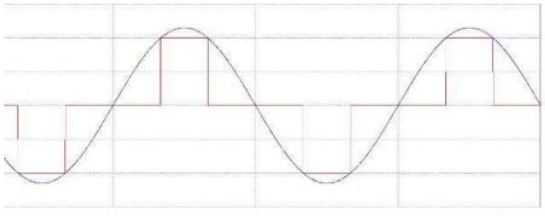


Fig:2.2 Output voltage wave form of an H-bridge inverter

| | S1 | S2 | S3 | S4 |
|---|---|---|---|---|
| 0 | 1 | 1 | | |
| Vdc | 1 | | | 1 |
| 0 | | | 1 | 1 |
| 0 | | | 1 | 1 |
| -Vdc | | 1 | 1 | |
| 0 | 1 | 1 | | |

TABLE 2.1 Switching table for H-Bridge

## 3.MULTILEVEL VOLTAGE SOURCE INVERTER USING CASCADED-INVERTERS WITH SEPARATED DC SOURCES

could not be met by the classical two-level inverter. Until recently, power transistors were slow, and their long turnon and off times The structure of the multilevel inverter using cascaded-inverters with separated dc sources will be introduced in this chapter, as well as switching pattern.

### 3.1 Introduction

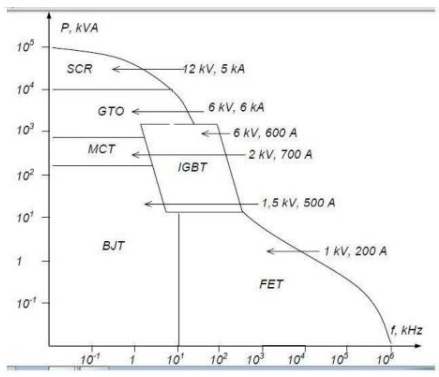
Multilevel inverters have been developed over the last three decades for the purpose of meeting the drive high voltage rating and low dv/dt value requirements that resulted in excessive switching losses that constrained the switching frequency to several kHz values. Also the voltage blocking capability of power transistors was below a kilovolt that implied such switches could not be utilized in two-level inverters at high voltage levels and could not be operated at switching frequencies in the tens of kilohertz range.

### 3.1.1 Introduction

GTO In the early 1980's utilizing darling ton power transistors and Gate Turn Off Thyristors (GTOs), the three-level NPC inverter could provide effectively quadrupled switching frequency and could provide high inverter voltage ratings (twice that of the two-level inverter). As a result, power and voltage levels above that of two-level inverter could be reached and the three-level NPC inverter has found immediate application in traction drives and industrial drives.

### 3.1.2 Introduction

IGBT In the 1990's, the IGBT was introduced as a fast turn-on, fast turn-off device that provided significant switching loss reduction and also the secondary breakdown of the Bipolar Junction Transistor (BJT) was absent.




### 3.2 TYPES OF Multilevel inverters

Multilevel inverter topologies often provide an output waveform with a nearly sinusoidal frequency and voltage, minimal harmonics, decreased common mode voltage, and low dv/dt, making them motor-friendly. The fundamental idea behind all multilevel inverter topologies, despite the variety of topology types, is to use multistage DC capacitor voltage levels in conjunction with low voltage rating power transistors in series connection to achieve higher output voltage levels in tiny incremental steps.

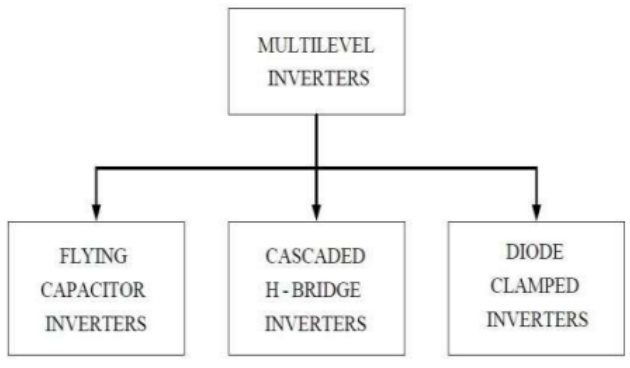



Fig: 3.1 Multilevel inverter topologies.

## 4. HARMONICS

### 4.1 WHAT IS A HARMONIC?

"A sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency" is the standard definition of a harmonic. [1]. Some sources define "clean" or "pure" power as having no harmonics. However, clear waveforms like this are usually seen in a laboratory. Harmonics are here to stay and have been for a very long time. Actually, from the creation of the first string or woodwind instrument, musicians have

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940

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Vol 18, Issue.2, 2024

been aware of such. What makes a clarinet sound like a clarinet and a trumpet sound like a trumpet is harmonics, sometimes referred to as "overtones" in music. Electrical generators aim to generate electricity in situations when the voltage waveform exhibits a single frequency, known as the fundamental frequency.
This frequency, or cycles per second, is 60 Hz in North America. The standard frequency for this frequency in Europe and other areas of the globe is 50 Hz. 400 Hz is often used as the fundamental frequency in aircraft. At 60 Hz, the voltage waveform rises to its greatest positive value, falls to zero, rises to a maximum negative value, and falls back to zero sixty times per second. Figure 1 illustrates the trigometric function known as a sine wave, which represents the pace at which these changes take place. Numerous natural phenomena, like the speed at which a pendulum swings back and forth or the way a violin string vibrates when it is plucked, exhibit this function.

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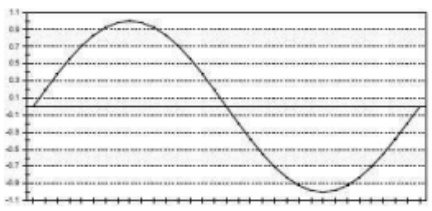

Fig.4.1 Sine wave

### 4.2 WHY WORRY ABOUT THEM?

Harmonics don't always indicate that the office or factory can't function correctly. It is dependent on the equipment's susceptibility and the "stiffness" of the power distribution system, much as other power quality problems. High harmonic voltage and/or current levels may cause a variety of equipment types to malfunction or fail, as the list below illustrates. Furthermore, a plant that is capable of operating correctly might be the cause of excessive harmonics. Harmonic pollution may have an impact on facilities on the same system that are more vulnerable because it is often transferred back into the electric utility distribution system.

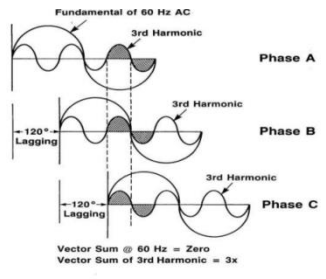


Fig.4.2 Additive Third Harmonics

| HARMONIC | FUND | 2ND | 3RD | 4TH | 5TH | 6TH | 7TH | ETC |
|---|---|---|---|---|---|---|---|---|
| SEQUENCE | + | - | 0 | + | - | 0 | + | ..... |

Table.4.1 Harmonic Sequencing Values in Balanced Systems

## 5.PROPOSED CASCADED H-BRIDGE MULTILEVEL INVERTER

Basically, the power circuit configuration of a CHB MLI, shown in figure 1, is a series connection of H-bridge inverter unit cells. Each of the H-bridge cells has a capacitor bank

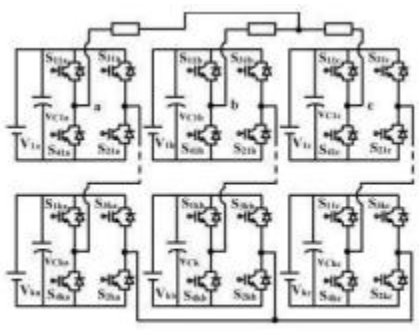

Fig:5.1 Cascaded H-bridge multilevel inverter power circuit

| Compared parameter | Modulation scheme | |
|---|---|---|
| | PS PWM | Proposed scheme |
| Number of triangular carriers per phase | 2N | 1 |
| Number of modulating signals per phase | 1 | 2 |
| Algorithm execution time (μs) | 2.85 | 2.62 |

Table:5.1 Comparison of phase-shift (PS) and proposed spwm schemes

It can then be inferred from table 1 that the overall inverter output voltage for k cascaded units in phase a is given by

$$\sum_{j=1}^{k} v_{aj} = V_{dc} \sum_{j=1}^{k} (g_{1j} - g_{3j}) .$$

### 5.1 PROPOSED SINGLE-CARRIER-BASED SPWM TEMPLATE

The suggested modulation method, as mentioned in the introduction, is a branch of IPD level-shifted SPWM in which the many triangular carrier signals are essentially represented by a single carrier. The continuous bands filled by these multi-triangular carriers in the conventional level-shifted SPWM are still apparent in this depiction.

because these bands are among the essential requirements for correctly stacking the waveforms that are generated from each series of H-bridges. The idea behind this modulation technique is to create a multilevel waveform template, or MWT, from which all of the H-bridge units' power switches are controlled. What's more intriguing is that, even though the deployed MWT formed from a phased-isposition level-shifted SPWM idea, the CHB inverter system can achieve equal power balancing among the contributing components. It is important to note that, as the literature has shown, modeling this MWT for any desired number of output voltage levels just requires the knowledge of certain facts of the CHB MLI setup. As a result, the block diagram in Figure 2 is followed by descriptions of the MWT creation for Phase A in the subsections that follow.

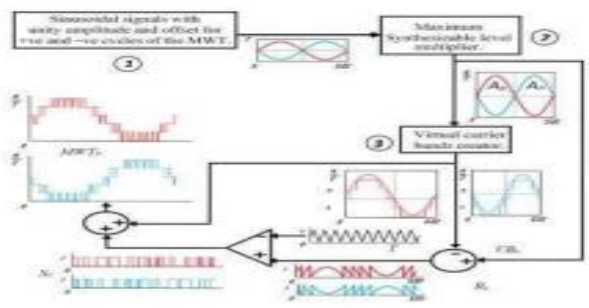

Fig:5.2 Per phase block diagram of the multilevel waveform template, MWT, generation

### 5.2 REFERENCE SIGNAL GENERATION

Among the basic waveforms required for the development of the MWT are sinusoidal signals. Figure 2 shows the blocks with the labels 1 and 2 where these waveforms are realized. Block 1 produces sine waves with a unity offset that are 180 degrees out of phase with one another. In light of the modulation technique that will be covered in subsequent portions of this work, the unity offset is necessary. [35] provided a generalized equation for the maximum number of phase-leg voltage levels, N, that could be synthesized in an MLI arrangement; this was shown in [36] as well. This phrase is repeated in this instance in (2).

$$N = \sum_{j=1}^{k} V_j (m_j - 1) .$$

## 6.THD COMPARISON OF MULTI-CARRIER PWM METHODS &SINGLE CARRIER PWM METHODS

### 6.1 MULTI-CARRIER PWM METHODS

For cascaded inverters, multi-carrier based PWM approaches are recommended. These techniques use several carriers, which may be sawtooth or triangular in shape [11]. In multi-carrier PWM strategies, the reference signal is often a sinusoidal signal or a system fault. This research focuses on the following multi-carrier PWM techniques

• PD-PWM

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN2454-9940

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Vol 18, Issue.2, 2024

• POD-PWM

### 6.1.1 PD-PWM In PDPWM

approach, many carriers are used in conjunction with a single reference signal. The carriers are grouped to produce coordinated voltage levels, and the carrier waveforms' phase information is the same. The PDPWM configuration for a cascading inverter's five voltage level switching is shown in the figure. It is clear that, in presentation form, the carrier frequency is 500 Hz and the modulation index is equal to 1. Carrier 1 is the source of S1–S4 switching signals. Carrier 2 is used to produce S2-S3 switching signals. The S5–S8 switching signals are produced by Carrier 3. Additionally, Carrier 4 generates the S6–S7 switching signals.

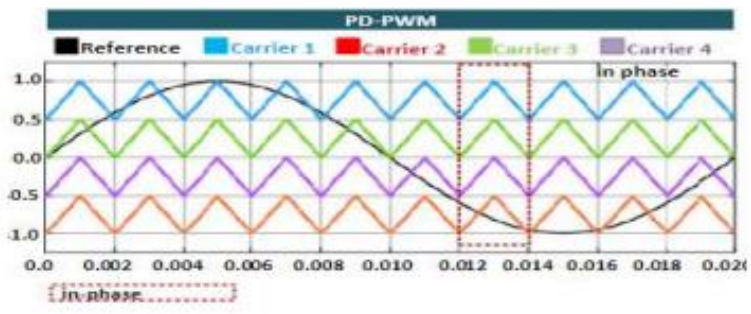


Fig.6.1. The modulation strategy of PD-PWM

## 7.SIMULATION RESULTS

### 7.1.SIMULATION CIRCUITS

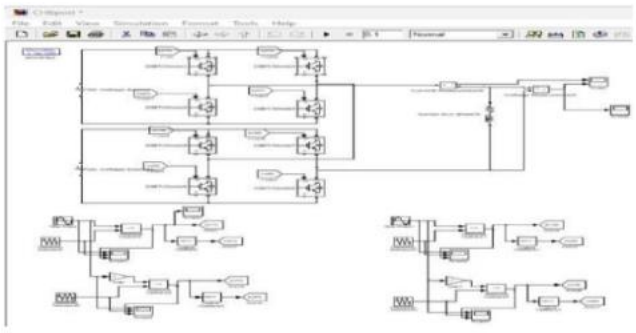

Fig:7.1 Simulink model of Phase Opposition Disposition PWM technique

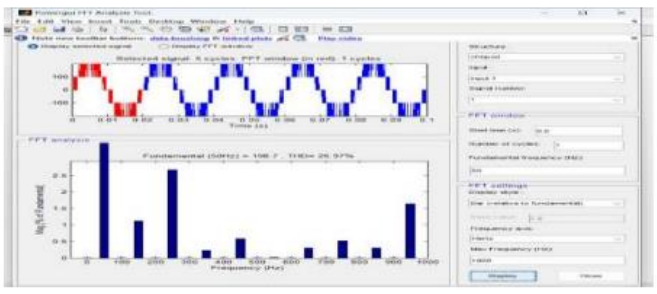

Fig:7.2 THD% of Phase Opposition Disposition PWM technique.

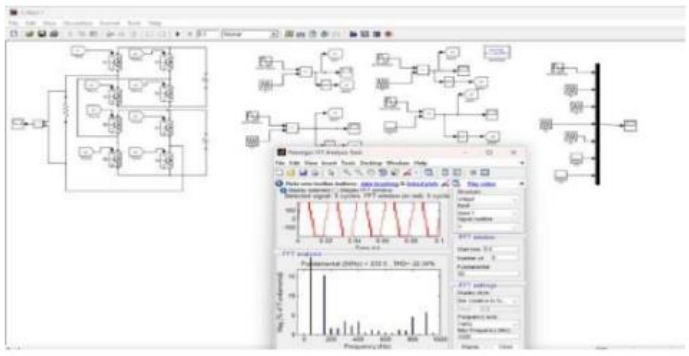

Fig:7.3 Simulink model & THD% of Phase Disposition PWM technique.

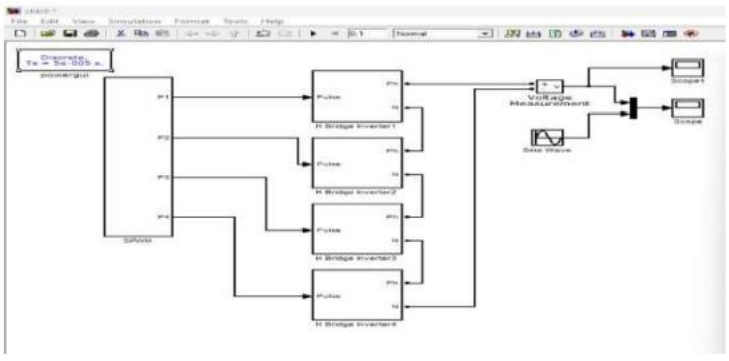

Fig:7.4 Simulink model of 9-level CHB MLI

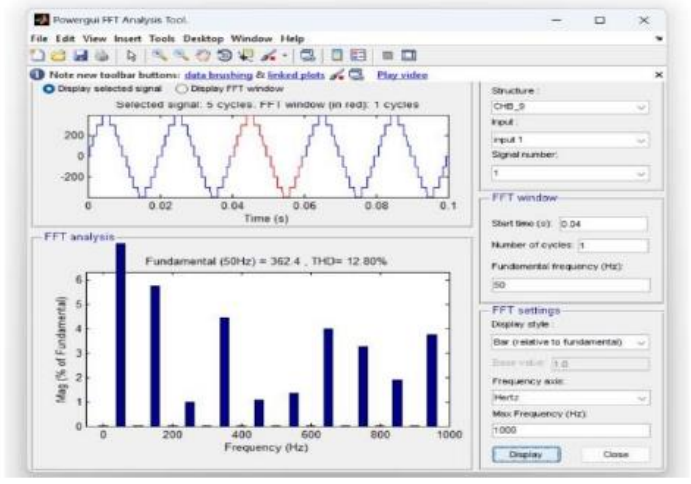


Fig:7.5 THD% of 9-level CHB MLI.

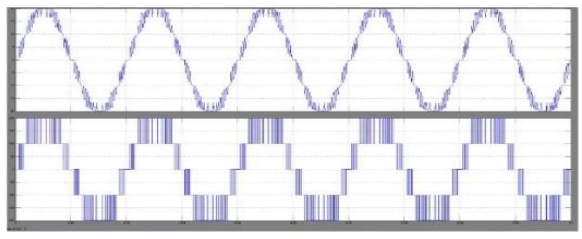

Fig:7.6 Output waveforms of Phase Opposition Disposition PWM technique.

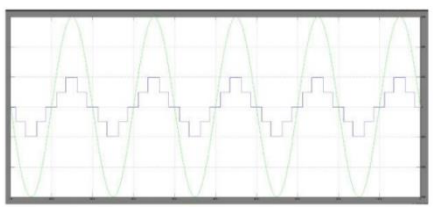

Fig:7.7 Output waveforms of Phase Disposition PWM technique.

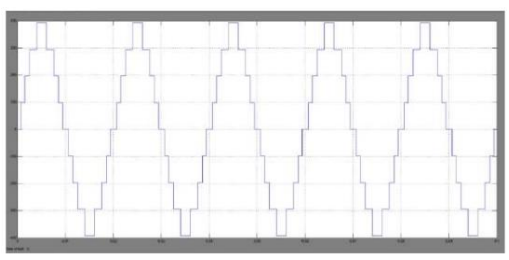

Fig:7.8 Output waveforms of 9-level CHB MLI.

## 8.CONCLUSION

A hybridized single carrier-based pulse width modulation technique for cascading H-bridge multilevel inverters is presented in this study. Its working principle has been thoroughly described. To create the intended output waveform template for the MLI, a sinusoidal modulating waveform is adjusted to fit within a single carrier signal range. The generation of the modulating templates follows a well-established modulation technique that was previously used for multilevel inverters. It has been shown that the creation of the modulating templates demonstrates how the well-known bipolar PWM may be extended to multi-cascaded H-bridge units. Without requiring any further control adjustment, the templates may be utilized on CHB inverters of any level once they are produced. From an industrial perspective, the MWT concept that is being presented will find use in many cascaded H-bridge systems because, as the number of inverter levels increases, the proposed modulation makes the inverter control system less sensitive to the conventional idea of

multiplicity of carrier waves. This will be very helpful since the control method will avoid the additional control work required for carrier synchronization. By using a reverse-voltage-sorting comparison method, the suggested SPWM makes sure that the switching pulses are distributed almost evenly across the power switches that make up the system. As a result, the true power fluctuations across the cascaded H-bridges are contained in a relatively small range. Our research indicates that the suggested control strategy produces a hybrid modulation scheme that mediates between the benefits of both the phase- and level-shifted carrier-based SPWM approaches. Through tests and scaled-down simulations on a 9-level CHB inverter, the performance of the suggested SPWM scheme has been shown; the findings have been presented in an appropriate manner.

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