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E-Mail :
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Verilog Implementation of a Vending Machine for Three Products Utilizing FSM Architecture

Aakula Lavanya[1], Dr. A. Nagaraju[2]

[1] IMS Solutions, Tarnaka, Hyderabad, Telangana, India

[2]Professor, Malla Reddy Institute of Technology and Science , Maisamma guda, Hyderabad Telangana, India

Abstract

The central idea of this work is the design and implementation of a vending machine capable of dispensing three products: candy, cake, and cool drinks. The vending machine operates using a Finite State Machine (FSM) architecture, which manages the sequence of operations including product selection, coin insertion, payment validation, product dispensing, and change return. The design emphasizes power efficiency through various reduction techniques and is implemented using Verilog HDL and Xilinx ISE 14.7, targeting the XC3S500E FPGA. Simulation results demonstrate the machine's ability to handle multiple coin denominations, accurately dispense products, and return change as necessary. The proposed system not only enhances user experience but also serves as a foundation for future enhancements, such as support for additional products and payment methods.

Keywords: Vending Machine, Finite State Machine (FSM), Verilog HDL, FPGA, Power Efficiency, Coin Insertion, Product Dispensing, Change Return, Digital Design.

I. Introduction

1.1 Introduction

This project is divided into two parts: the fundamental aspects related to the design of the vending machine controller and additional features that enhance its functionality. The design employs a Finite State Machine (FSM) architecture, which is essential for managing the various states of the vending machine. The FSM consists of ten states, requiring four bits for encoding. The simulation results demonstrate the machine's ability to handle multiple coin insertions and dispense products accordingly. Future enhancements may include additional features such as handshake signals to increase transaction security.

1.2 Objective

The objective of this project is to design and implement a three-product vending machine using FSM architecture in Verilog HDL. The system autonomously manages the full sequence of operations involved in a vending transaction, including product selection, coin insertion, payment validation, product dispensing, and change return. The FSM is designed using synchronous logic, ensuring reliable and efficient operation suitable for real-time embedded applications.

1.3 Organization

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The Verilog design is organized around a defined set of states: IDLE, SELECT_PRODUCT, WAIT_FOR_MONEY, DISPENSE_PRODUCT, RETURN_CHANGE, and ERROR_STATE. The machine starts in the IDLE state, transitions through various states based on user inputs, and utilizes a case statement to describe FSM transitions. The design encapsulates a top-level vending machine module with internal registers to hold the current state, next state, selected product, and accumulated money.

II: Literature Review

The literature review highlights various studies related to low-power design techniques and efficient implementations of digital systems. Notable works include the design of BCD adders and power consumption analysis on FPGA platforms. These studies provide insights into optimizing digital designs for performance and efficiency, which are relevant to the vending machine project.

III: Existing System

The existing vending machine systems typically operate with limited functionality, accepting specific coin denominations and dispensing products based on exact amounts. The proposed system enhances this by allowing for combinations of coins and providing change, thus improving user experience.

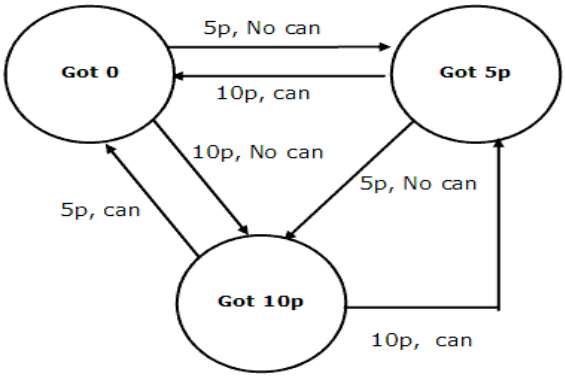

Fig Diagram of Vending machine using mealy model

States: S0: Got 0, S1: Got 5p, S2: Got 10p

Inputs: I5: 5p inserted I10: 10p inserted

Outputs (tuple notation): 0: Nothing,01: Dispense Can, 02: Dispense Can + Return

5p

IV: Proposed System

The proposed vending machine accepts two types of coins (₹5 and ₹10) and supports three products with the following prices:

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S.No	Product	Price
1	Candy	5
2	Cake	10
3	Cool drink	15

Fig 4.1 : Block diagram of vending machine

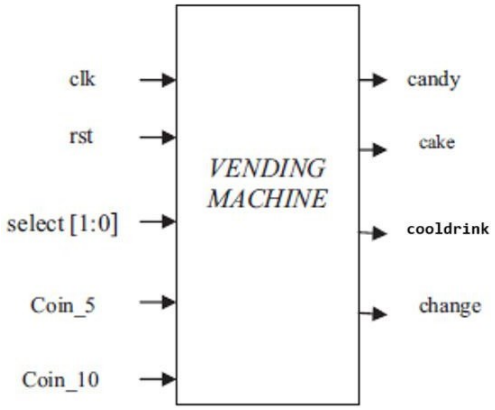

Fig 4.1 : Block diagram of vending machine

The system's FSM is designed to handle product selection, coin insertion, and change return effectively.

From the figure 1 it is clear that vending machine only accepts two types. of coins i.e. coinB5 (for a 5 rupee coin) and coinB10 (for a 10 rupee coin). Four types of select bit are also present for the user i.e.

- SB0: initially it will be present in idle state or reset state.
- SB1 (2Γb01): for the selection of product candy.
- SB2 (2Γb10): for the selection of the product cake.
- SB3 (2Γb11): for the selection of the product cooldrink.

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Vending machine has also five intermediate states.

- StB0(if it is in state zero)
- StB5(if it is in state five)
- StB10(if it is in state ten)
- StB15(if it is in state fifteen)
- StB20(if it is in state twenty)

the FSM of cooldrink, candy, cake are shown in figure 4.2, 4.3 and 4.4 respectively.

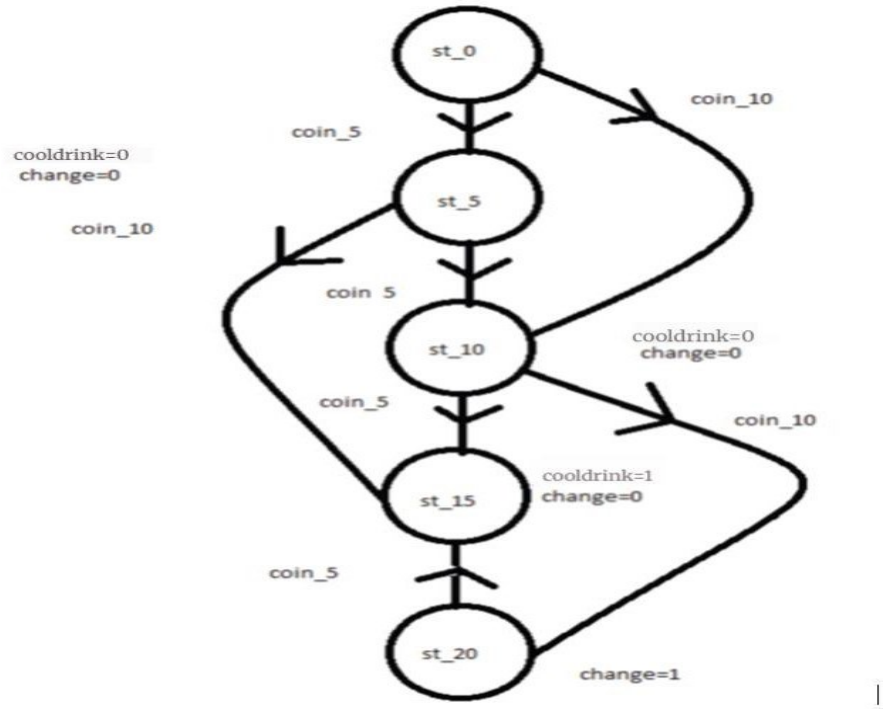

Fig 4.2 : FSM for cooldrink

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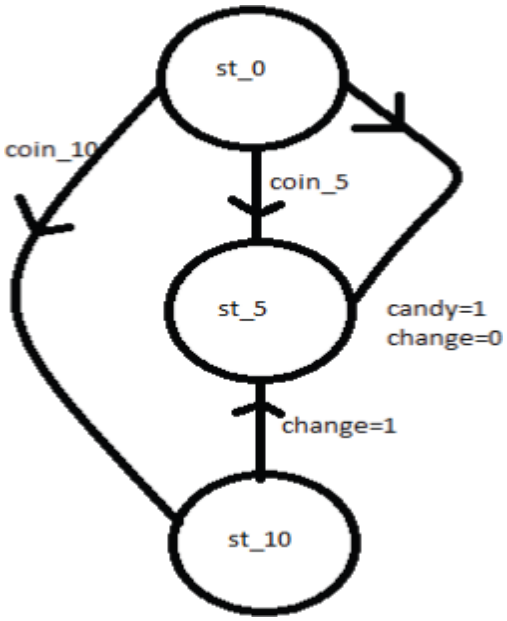

Fig 4.3 : FSM for candy

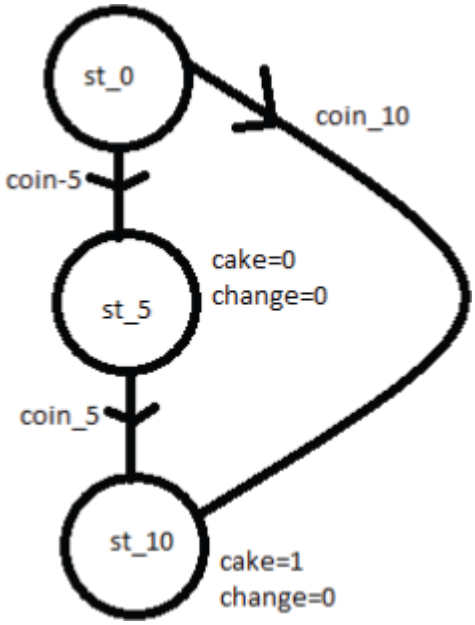

Fig 4.4 : FSM for cake

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V: System Requirements

The design utilizes Xilinx ISE for synthesis and implementation. The Verilog code is structured to facilitate easy simulation and testing. The synthesis process transforms the HDL code into a gate-level netlist, which is essential for FPGA implementation.

5.1 Introduction to Verilog

Verilog is a widely used hardware description language that allows designers to model digital systems at various levels of abstraction. Its syntax is similar to the C programming language, making it accessible for those with programming experience.

5.2 Program Structure

The basic unit in Verilog is the module, which contains declarations for inputs, outputs, and internal signals. The module structure allows for clear organization and readability of the design.

VI: Results and Discussions

The RTL schematic and technology schematic provide insights into the design's performance and resource utilization. Simulation results confirm the correct operation of the vending machine, demonstrating its ability to dispense products and return change accurately.

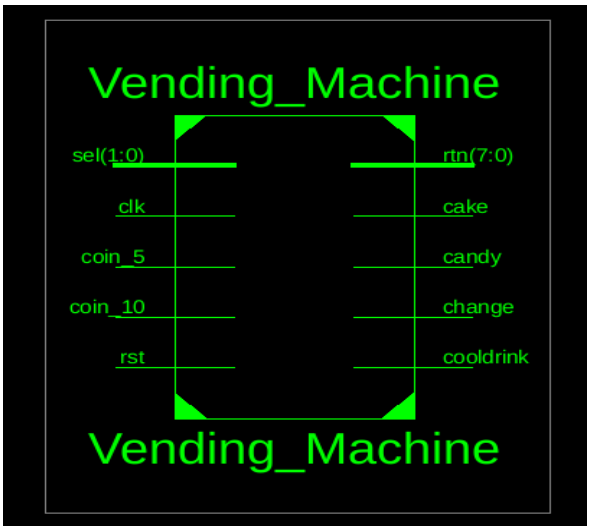

Fig 6.1: RTL Schematic of turbo encoder

RTL SCHEMATIC:

RTL schematic is described as register transfer logic that means the logic is transferred to registers it is also known as designer view because of it is looking like what is the intension of designer.

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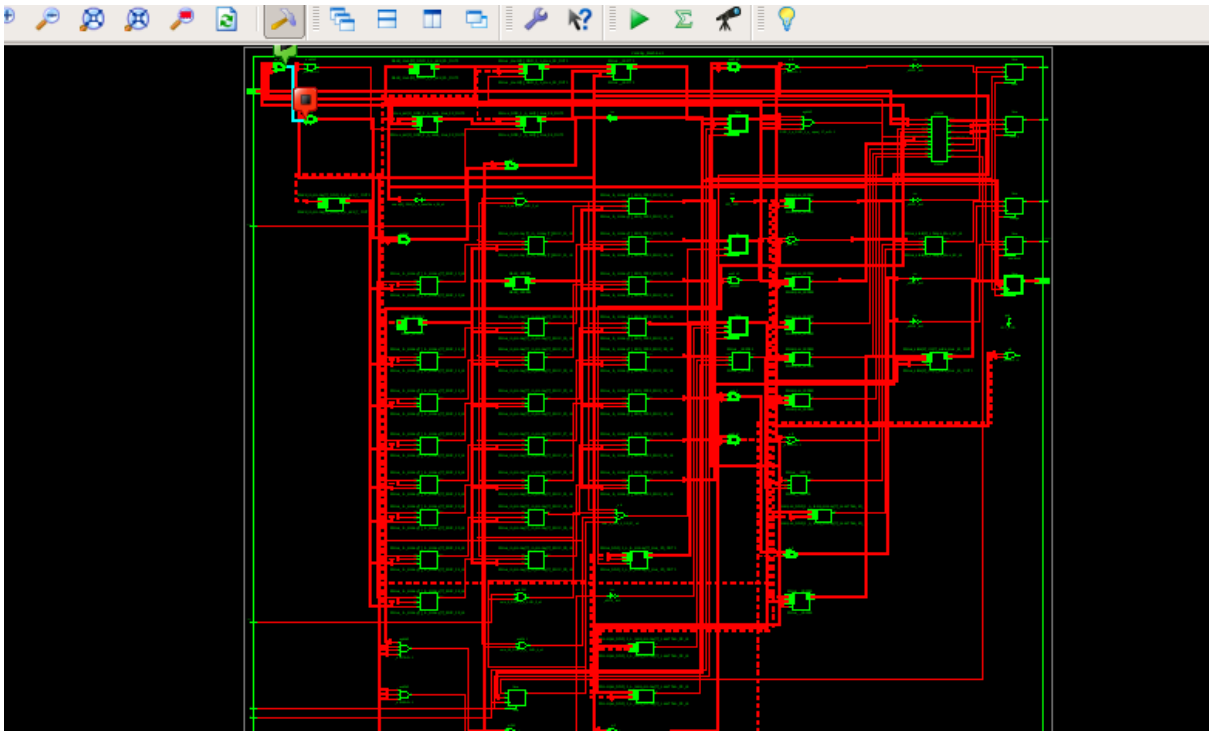

Fig 6.2: View technology schematic of turbo encoder

Displays the gate-level implementation after synthesis, including standard cells like NAND, NOR gates.
Useful for analyzing actual hardware realization and estimating area, timing, and power.

The technology schematic makes the representation of the architecture in the LUT format, where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design. the LUT is consider as an square unit the memory allocation of the code is represented in there LUT s in FPGA.

6.1 RTL Schematic

The Register Transfer Level (RTL) schematic of the vending machine design illustrates the interconnections between registers, multiplexers, and combinational logic. The RTL representation provides a high-level view of how data flows through the system, highlighting the key components involved in the vending machine's operation. The schematic confirms that the design adheres to the intended functionality, with clear pathways for data transfer and control signals.

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6.2 Technology Schematic

The technology schematic represents the gate-level implementation of the vending machine after synthesis. It includes standard cells such as NAND and NOR gates, which are essential for realizing the logic functions defined in the Verilog code. This schematic is crucial for analyzing the actual hardware realization of the design, allowing for estimations of area, timing, and power consumption. The technology schematic confirms that the design is optimized for the target FPGA, ensuring efficient use of resources.

6.3 Simulation Results

Simulation plays a vital role in verifying the functionality of the vending machine design. The simulation results demonstrate the system's responsiveness to user inputs and its ability to execute the defined state transitions accurately. The following key scenarios were tested:

- Inserting a 5-Rupee Coin for Candy: The simulation confirmed that when a 5-rupee coin was inserted, the machine correctly transitioned to the appropriate state, indicating that the amount collected was insufficient for the selected product. The system prompted for additional coins.

- Inserting a 10-Rupee Coin for Cake: When a 10-rupee coin was inserted for the cake selection, the machine successfully transitioned to the state indicating that the required amount was met. The simulation verified that the cake was dispensed, and the system returned to the idle state.

- Inserting Coins for Cool Drink: The simulation illustrated the machine's ability to handle multiple coin insertions. For instance, when a user inserted a 5-rupee coin followed by a 10-rupee coin for a cool drink, the machine correctly calculated the total amount and dispensed the product while returning the appropriate change.

6.4 Performance Metrics

The performance metrics obtained from the synthesis and simulation of the design are summarized in Table 6.1. These metrics provide insights into the efficiency and effectiveness of the vending machine implementation:

Table 6.1: Hardware utilization summary

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Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	9	960	0%
Number of Slice Flip Flops	7	1920	0%
Number of 4 input LUTs	18	1920	0%
Number of bonded IOBs	10	66	15%
Number of GCLKs	1	24	4%

Minimum period	2.928 ns
Maximum Frequency	341.565MHz
Minimum input arrival time before clock	3.562ns
Maximum output required time after clock	5.255ns
Maximum combinational path delay	5.895ns

Minimum Period: The minimum period of 2.928 ns indicates the fastest clock cycle the design can support, translating to a maximum frequency of 341.565 MHz. This high frequency ensures that the vending machine can respond quickly to user inputs.

Input and Output Timing: The timing metrics for input arrival and output requirements demonstrate that the design meets the necessary timing constraints for reliable operation. The minimum input arrival time before the clock and maximum output required time after the clock are within acceptable limits, ensuring that the system operates smoothly without timing violations.

6.5 Discussion of Results

The results obtained from the simulation and synthesis of the vending machine design validate the effectiveness of the FSM architecture in managing the various states and transitions required for a functional vending machine. The design successfully handles multiple coin denominations, accurately dispenses products, and returns change as needed.

The use of Verilog HDL for implementation allowed for a clear and structured approach to designing the vending machine. The modular nature of the code facilitated easy debugging and testing, ensuring that each component of the system functioned as intended. The simulation results confirmed that the design met the specified requirements, providing a reliable and efficient solution for a three-product vending machine.

Furthermore, the power efficiency techniques employed in the design contribute to its overall effectiveness, making it suitable for real-world applications where energy consumption is a critical factor. The successful implementation of the vending machine serves as a foundation for future enhancements, such as the integration of additional products, support for currency notes, and improved user interfaces.

The results demonstrate that the Verilog implementation of the vending machine using FSM architecture is both functional and efficient, providing a solid basis for further exploration and development in digital design and embedded systems.

VII: Conclusion and Future Enhancement

7.1 Conclusion

The proposed vending machine design effectively addresses the limitations of existing systems by allowing for flexible coin insertion and change return. This enhances user experience and operational efficiency.

7.2 Future Enhancement

Future work may include the integration of additional features such as support for currency notes, enhanced security measures, and the ability to handle more complex transactions. The project lays a strong foundation for further exploration in digital design and embedded systems.

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This publication matter provides a comprehensive overview of the Verilog implementation of a vending machine using FSM architecture, suitable for submission to a conference or journal in the field of digital design and embedded systems.