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High-Performance Mixed-Logic Approach to Low Power 2–4 and 4–16 Line Decoder Circuits

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Abstract - This summary outlines a novel line decoder design strategy that utilizes a hybrid logic approach. The methodology integrates transmission gate logic, pass transistor dual-value logic, and conventional static CMOS logic. For the 2-to-4 decoder, two innovative configurations are introduced: one employing 14 transistors, optimized for minimal transistor usage and reduced power consumption, and another using 15 transistors, designed to enhance power-delay performance. Each configuration supports both fixed function and adaptive modes, resulting in four distinct decoder variants. Additionally, four new 4-to-16 decoders are developed using a hybrid framework that combines 2-to-4 pre decoders with traditional CMOS post-decoders. Compared to conventional CMOS designs, the proposed decoders offer higher output swing and require fewer transistors. Simulation results using a 32 nm technology node demonstrate notable improvements in both power efficiency and delay characteristics.

Keywords: Hybrid Logic Design, Line Decoder, Transmission Gate Logic, Pass Transistor Dual-Value Logic, Static CMOS Logic.

INTRODUCTION TO VLSI

VLSI stays for "Generous Scale Integration". This is the field which incorporates squeezing progressively justification devices into smaller and more diminutive regions. VLSI, circuits that would have devoured boardfuls of room would now have the capacity to be put into a little space couple of millimeters over! This has opened up a noteworthy opportunity to do things that were improbable beforehand. VLSI circuits are everywhere .your PC, your auto, your new out of the plastic new best in class modernized camera, the cell phones, and what have you. This incorporates a lot of expertise on various fronts inside a comparative field, which we will look at in later portions. VLSI has been around for a long time, yet as a response of advances in the domain of PCs, there has been a passionate extension of contraptions that can be used to diagram VLSI circuits. Close by, conforming to Moore's law, the limit of an IC has extended exponentially consistently, to the extent computation control, utilization of available domain, yield. The combined effect of these two advances is that people would now have the capacity to put diverse helpfulness into the IC's, opening up new unsettled areas. Models are introduced structures, where smart devices are put inside normal things, and ubiquitous handling where small enrolling contraptions increase to such an extent, to the point that even the shoes you wear may truly achieve something supportive like checking your heartbeats. Facilitated circuit (IC) development is the engaging advancement for a whole host of creative devices and structures that have changed the way in which we live. Jack Kilby and Robert Noyce got the 2000 Nobel Prize in Physics for their production of

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the joined circuit; without the organized circuit, neither transistors nor PCs would be as basic as they are today. VLSI systems are extensively humbler and exhaust less power than the discrete sections used to build electronic structures beforehand the 1960s. Blend empowers us to fabricate structures with various more transistors, empowering essentially all the more enrolling ability to be associated with dealing with an issue. Composed circuits are furthermore considerably less requesting to plan and make and are more reliable than discrete systems; that makes it possible to make exceptional reason structures that are more viable than comprehensively helpful PCs for the activity that should be finished.

INTRODUCTION TO DECODERS

STATIC cmos circuits are used for most by a long shot of basis doors in fused circuits They involve complemen-tary N - type metal-oxide-semiconductor (nMOS) pulldown and P-type metal-oxide semiconductor (pMOS) pullup frameworks and present incredible execution and also security from confusion and contraption assortment. Thusly, essential metal-oxide semiconductor (CMOS) method of reasoning is depicted by quality against voltage scaling and transistor estimating and thusly tried and true assignment at low voltages and little transistor sizes [2]. Data signals are related with transistor entryways simply, offering decreased diagram versatile quality and help of cell-based method of reasoning mix and plan.

Pass transistor reason (PTL) was basically made in the 1990s, when diverse diagram styles were familiar pointing with give an appropriate differentiating alternative to CMOS justification and im-show speed, power, and region. Its rule layout differentiate is that data sources are associated with both the gateways and the source/exhaust diffu-sion terminals of transistors. Line decoders are basic circuits, for the most part used as a piece of the periphery equipment of memory displays (e.g., SRAM). This short develops a mixed method of reasoning procedure for their execution, picking improved execution appeared differently in relation to single-style layout. Whatever is left of this brief is dealt with as takes after: Section II gives a short survey of the assessed decoder circuits, realized with consistent CMOS reason. Portion III in-troduces the new mixed method of reasoning blueprints. Zone IV drives a close multiplication look at among the proposed and con-ventional decoders, with a point by point chat on the surmised comes to fruition. Fragment V gives the blueprint and last completes of the work presented.

TABLE I
TRUTH TABLE OF THE 2–4 DECODER

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

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TABLE II
TRUTH TABLE OF THE INVERTING 2–4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

OVERVIEW OF LINE DECODER CIRCUITS

In advanced frameworks, discrete amounts of data are repre-sented by twofold codes. A n-bit parallel code can speak to up to 2n particular components of coded information. A decoder is a combina-tional circuit that proselytes parallel data from n input lines to a most extreme of 2n remarkable yield lines or less if the n-bit coded data has unused blends.

A. 2– 4 Line Decoder

A 2– 4 line decoder creates the 4 minterms D0−3 of 2 input factors An and B. Its method of reasoning movement is dense in Table I. Dependent upon the data mix, one of the 4 yields is picked and set to 1, while the others are set to 0. A changing 2– 4 decoder makes the fundamental minterms I0−3, consequently the picked yield is set to 0 and the rest are set to 1, as showed up in Table II. In conventional CMOS blueprint, NAND and NOR entryways are needed to AND or conceivably, since they can be realized with 4 transistors, rather than 6, likewise executing justification limits with higher adequacy. A 2– 4 decoder can be completed with 2 inverters and 4 NOR passages Fig. 1(a), while a changing decoder requires 2 inverters and 4 NAND entryways Fig. 1(b), both yielding 20 transistors.

B. 4– 16 Line Decoder With 2– 4 Predecoders

A 4– 16 line decoder delivers the 16 minterms D0−15 of 4input elements A, B, C, and D, and a switching 4– 16 line decoder creates the equal minterms I0−15. Such circuits can be completed using a predecoding procedure, as shown by which bits of n address bits can be predecoded into 1-of-2n predecoded lines that fill in as commitments to the last stage decoder [1]. Thusly, a 4– 16 decoder can be imple-mented with 2 2– 4 modifying decoders and 16 2-input NOR portals [Fig. 2(a)], and a changing one can be executed with 2 2– 4 decoders and 16 2-input NAND passages [Fig. 2(b)]. In CMOS method of reasoning, these layouts require 8 inverters and 24 2-input entryways, yielding an entirety of 104 transistors each

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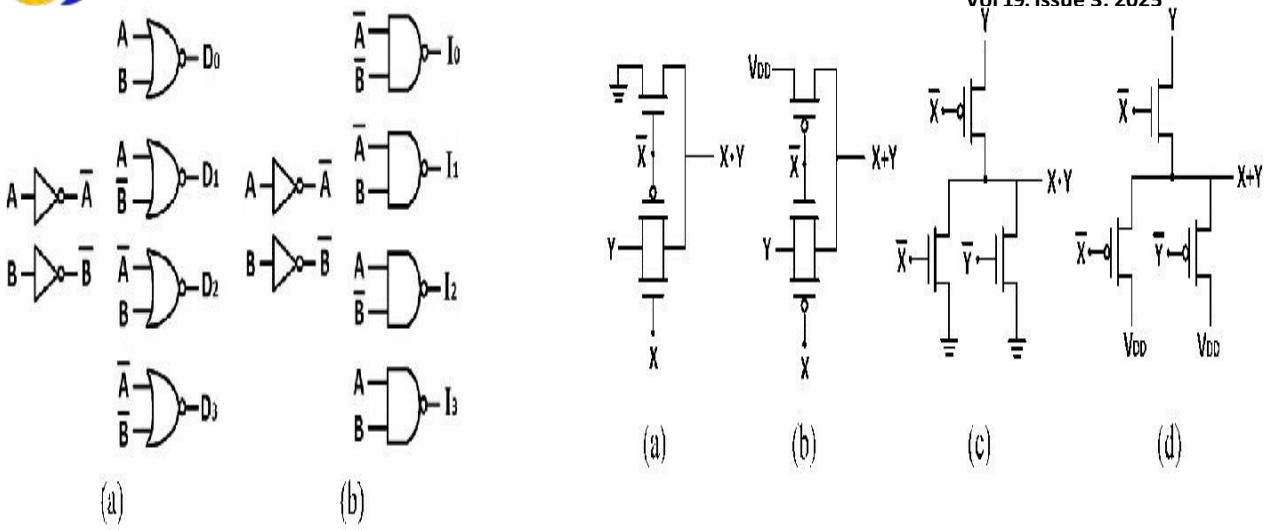

. 1. 20-transistor 2–4 line decoders implemented with CMOS logic. (a) Noninverting NOR-based decoder. (b) Inverting NAND-based decoder

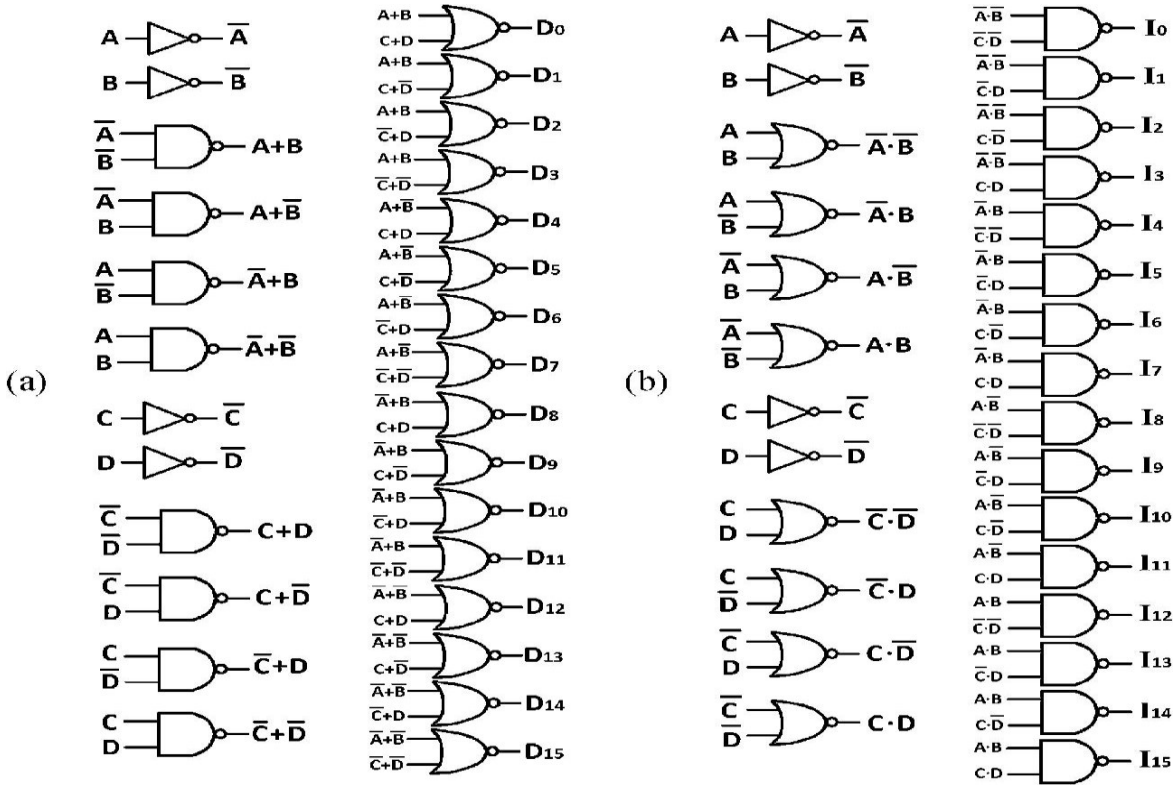

Fig. 2. 104-transistor 4–16 line decoders implemented with CMOS logic and predecoding. (a) Noninverting decoder implemented with two 2–4 inverting predecoders and a NOR-based postdecoder. (b) Inverting decoder implemented with two 2–4 noninverting predecoders and a NAND-based postdecoder.

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A. 14-Transistor 2– 4 Low-Power Topology

Planning a 2– 4 line decoder with either TGL or DVL entryways would require an aggregate of 16 transistors (12 for AND/OR doors and 4 for inverters). Be that as it may, by blending both AND door composes into a similar topology and utilizing appropriate flag course of action, it is conceivable to dispose of one of the two inverters, in this manner diminishing the aggregate transistor tally to 14.

Give us a chance to accept that, out of the two data sources, in particular, An and B, we intend to wipe out the B inverter from the circuit. At long last, The D3 minterm (AB) is executed with a TGL door, hence, the B inverter can be wiped out from the circuit, bringing about a 14-transistor topology (9 nMOS and 5 pMOS).

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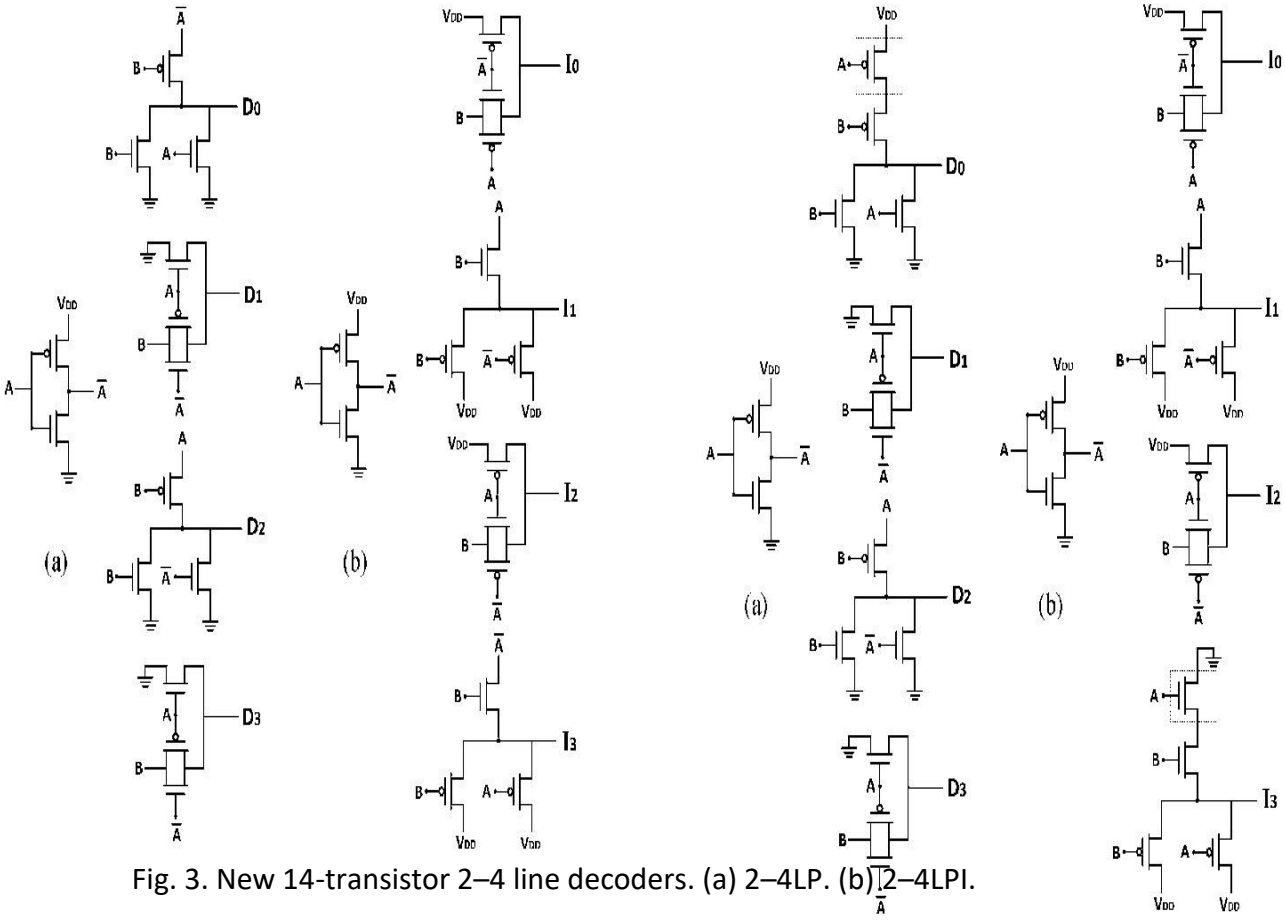

Fig. 3. New 14-transistor 2–4 line decoders. (a) 2–4LP. (b) 2–4LPI.

Following a comparable strategy with OR entryways, a 2– 4 reversing line decoder can be actualized with 14 transistors (5 nMOS and 9 pMOS) also: I0 and I2 are executed with TGL (us-

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ing B as the proliferate flag), and I1 and I3 are executed with DVL (utilizing An as the engender flag). The B inverter can by and by be omitted.

Inverter end lessens the transistor check, intelligent exertion and by and large exchanging action of the circuits, in this way diminishing force dispersal. The two new topologies are named "2– 4LP" and "2– 4LPI," where "LP" remains for "low power" and "I" for "altering." Their schematics are appeared in Fig. 4(a) and (b), individually.

B. 15-Transistor 2– 4 High-Performance Topology

The low-control topologies exhibited above have a downside in regards to most pessimistic scenario delay, which originates from the utilization of correlative An as the spread flag on account of D0 and I3. Notwithstanding, D0 and I3 can be productively actualized utilizing static CMOS doors, without utilizing integral sig-nals. In particular, D0 can be actualized with a CMOS NOR door and I3 with a CMOS NAND entryway, adding one transistor to every topology. The new 15T outlines present a huge change in delay while just marginally expanding power dissemination. They are named "2– 4HP" (9 nMOS, 6 pMOS) and "2– 4HPI" (6 nMOS, 9 pMOS), where "HP" remains for "superior" and "I" remains for "transforming." The 2– 4HP and 2– 4HPI schematics are appeared in Fig. 5(a) and (b), separately.

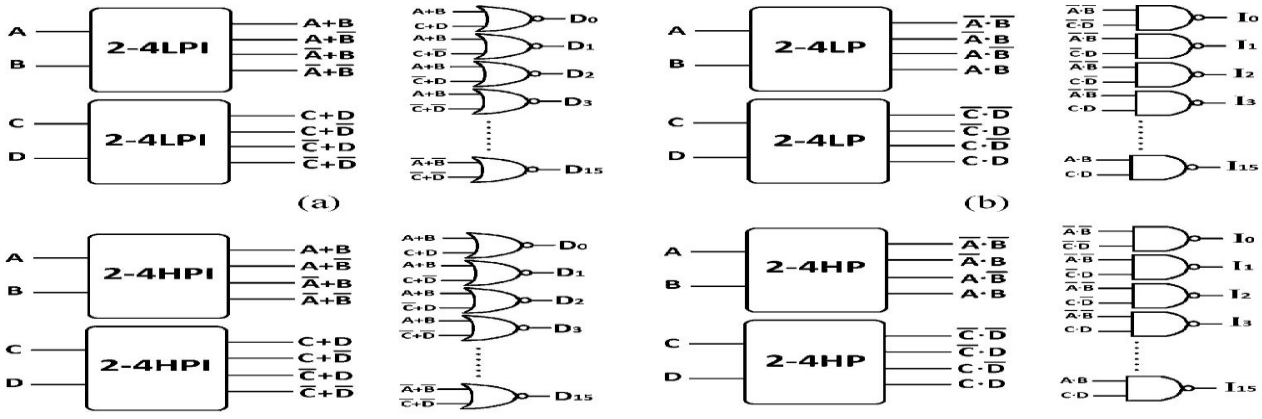

Fig.4. New 4–16 line decoders. (a) 4–16LP. (b) 4–16LPI. (c) 4–16HP. (d) 4–16HPI

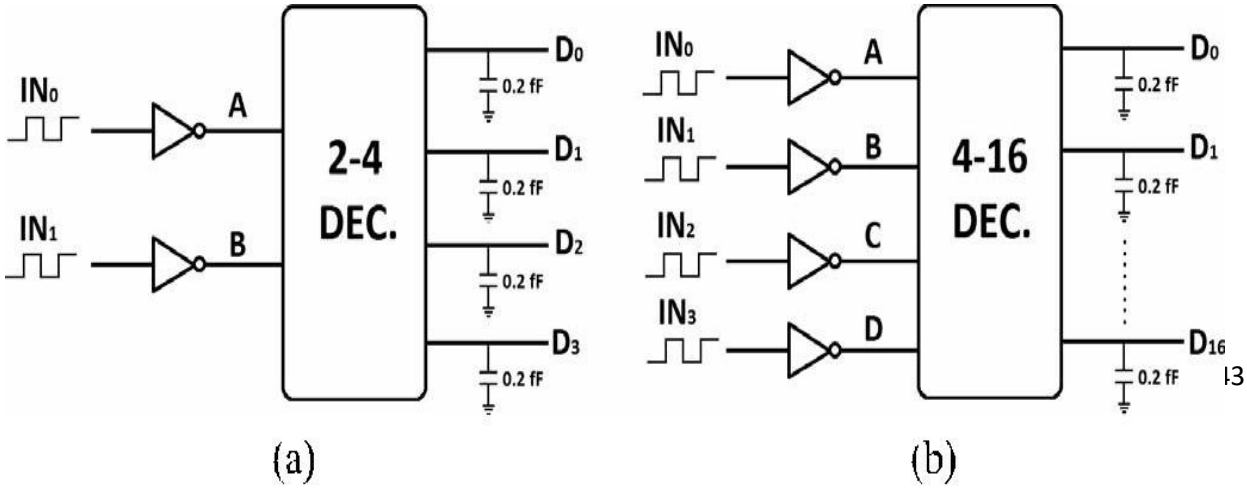

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Fig. 5. Simulation setup regarding input/output loading conditions. (a) 2–4 de-coders. (b) 4–16 decoder

SIMULATIONS

In this area, we play out an assortment of BSIM4-construct flavor recreations in light of the schematic level, keeping in mind the end goal to contrast the proposed blended rationale decoders and the ordinary CMOS. The circuits are actualized utilizing a 32 nm prescient tech-nology display for low-control applications (PTM LP), incor-porating high-k/metal door and stress impact [11]. For reasonable and fair-minded examination we utilize unit-measure transistors solely (Ln = Lp = 32 nm, Wn = Wp = 64 nm) for all decoders.

A. Recreation Setup

All circuits are recreated with fluctuating recurrence (0.5, 1.0, 2.0 GHz) and voltage (0.8, 1.0, 1.2 V), for a sum of 9 reenactments. Every reproduction is rehashed 5 times with shifting temperature (−50, −25, 0, 25, and 50 ◦C) and the normal power/delay is ascertained and exhibited for each situation. All in-puts are cushioned with adjusted inverters (Ln = Lp = 32 nm, Wn = 64 nm, Wp = 128 nm) and all yields are stacked with a capacitance of 0.2 fF, as appeared.

Moreover, legitimate piece arrangements are embedded to the in-puts, keeping in mind the end goal to cover every conceivable progress a decoder can perform. A 2– 4 decoder has 2 inputs, which can create 22 = 4 distinctive twofold blends, in this manner yielding an aggregate of 4 ∗ 4 = 16 conceivable changes. The 2– 4 decoders are reproduced for 64 nanoseconds (ns), with the goal that the 16-bit input successions are rehashed 4 times. Also, a 4– 16 decoder has 4 inputs, 42 = 16 input blends and 16 ∗ 16 = 256 conceivable advances, in this manner the 4– 16 decoders are reproduced for 256 ns to precisely cover all changes once. Fig. 8 delineates the information/yield wave-types of our proposed 2– 4 decoders for each of the 16 input advances, showing their full swinging capacity.

B. Execution Metrics Examined

The measurements considered for the correlation are: normal power dispersal, most pessimistic scenario deferral and power-postpone item (PDP). With persistent sub-micron scaling and low voltage task, spillage control has turned out to be progressively critical as it commands the dynamic one [12]. In our examination, both spillage and dynamic streams are viewed as and the aggregate power dispersal is separated from flavor recreation, estimated in nanowatts (nW).

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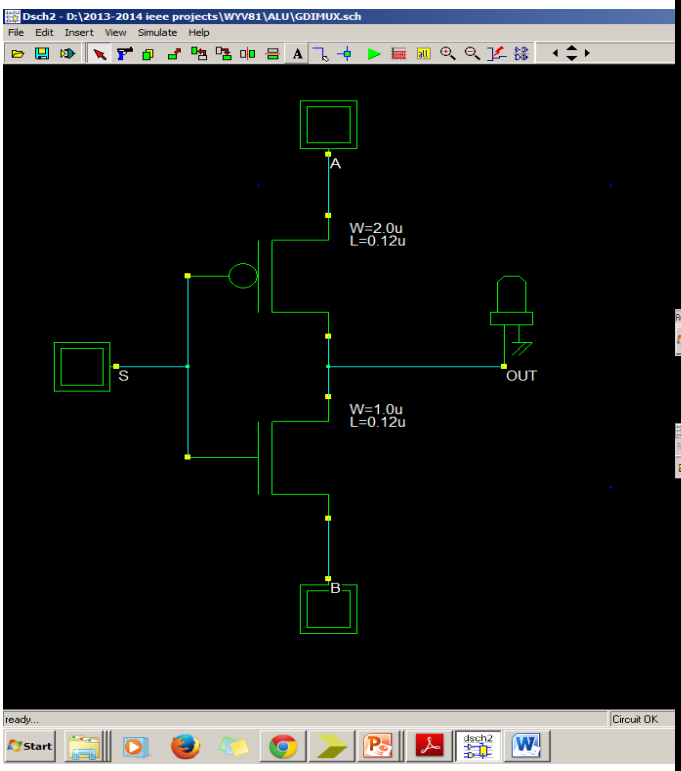
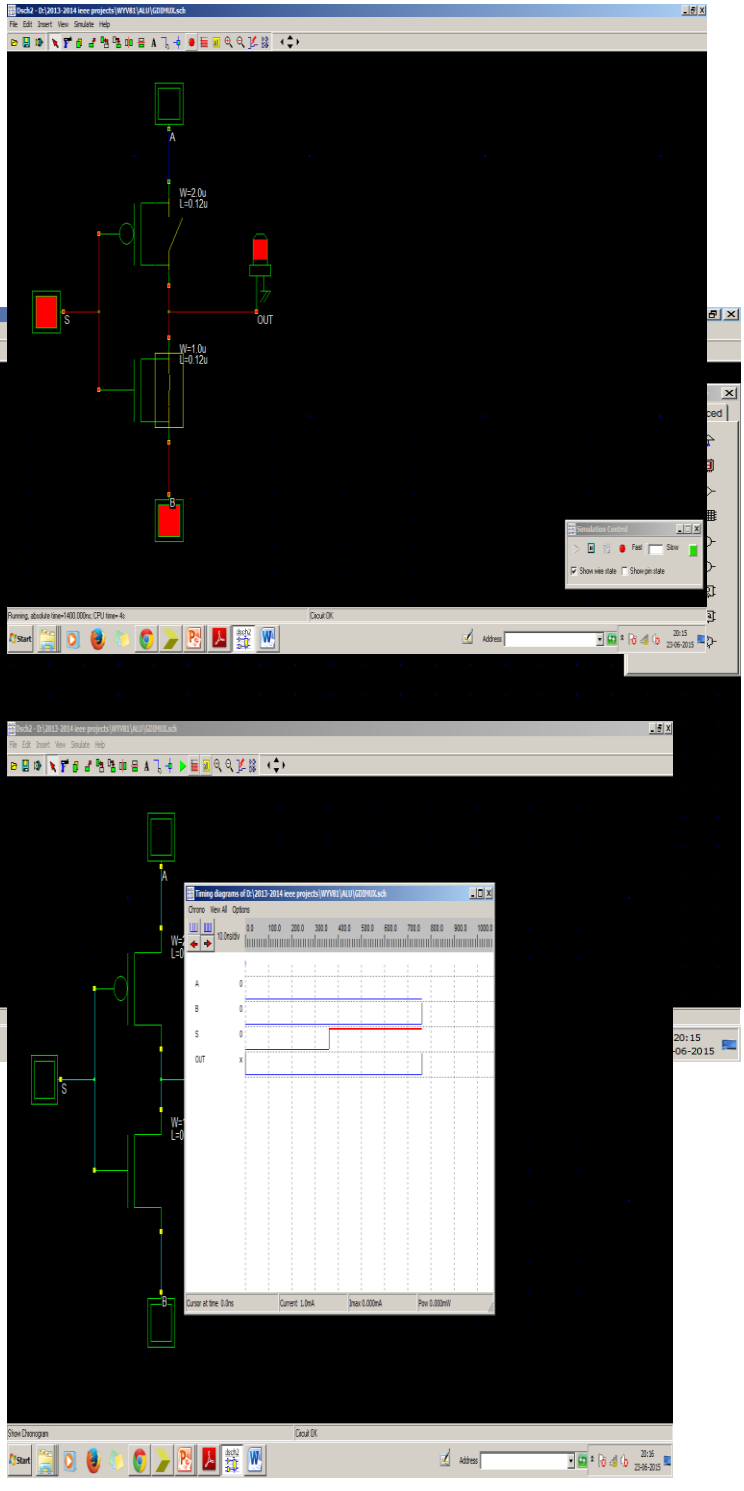
Concerning, we take note of the most elevated esteem that happens among all I/O advances, estimated in picoseconds (ps). At long last, PDP is assessed as normal power*max delay and estimated in electronvolts (eV).

Results and investigation:GDI_MUX:

Schematic:



Simulation:



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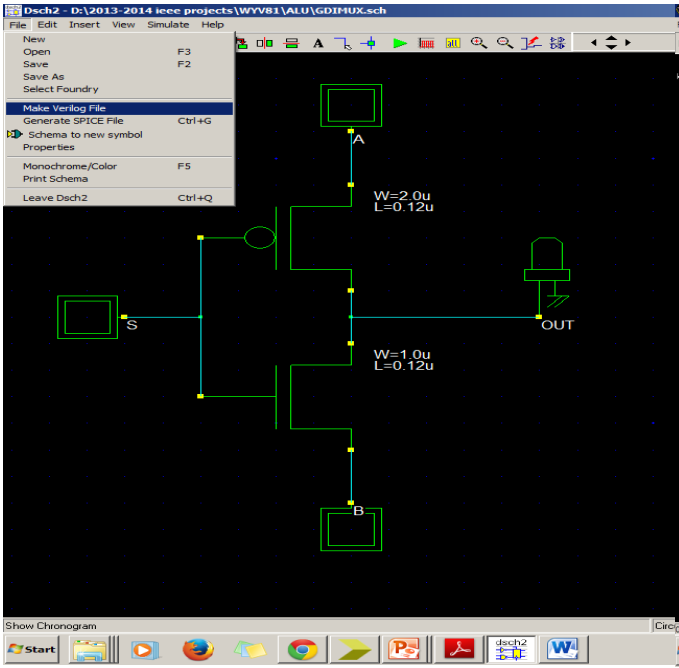
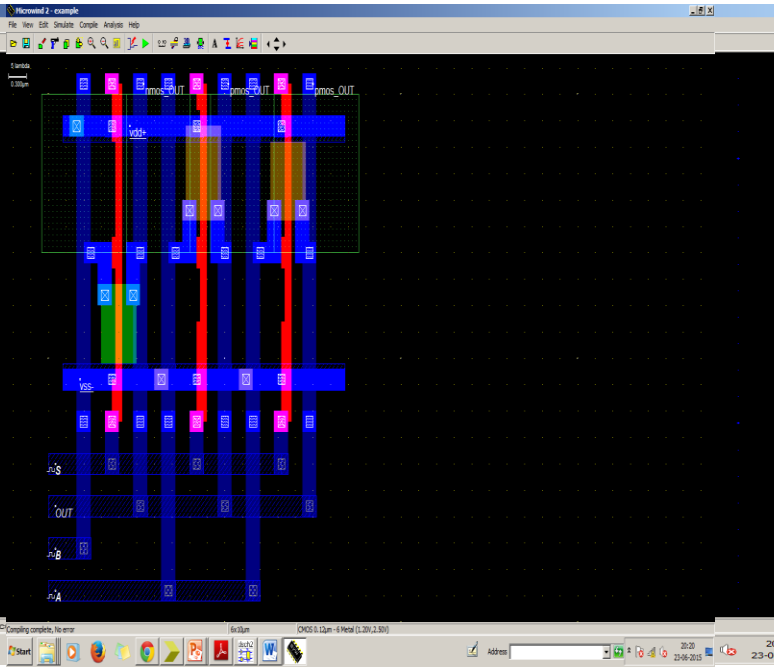
Making a Verilog file:



Layout of GDI MUX:



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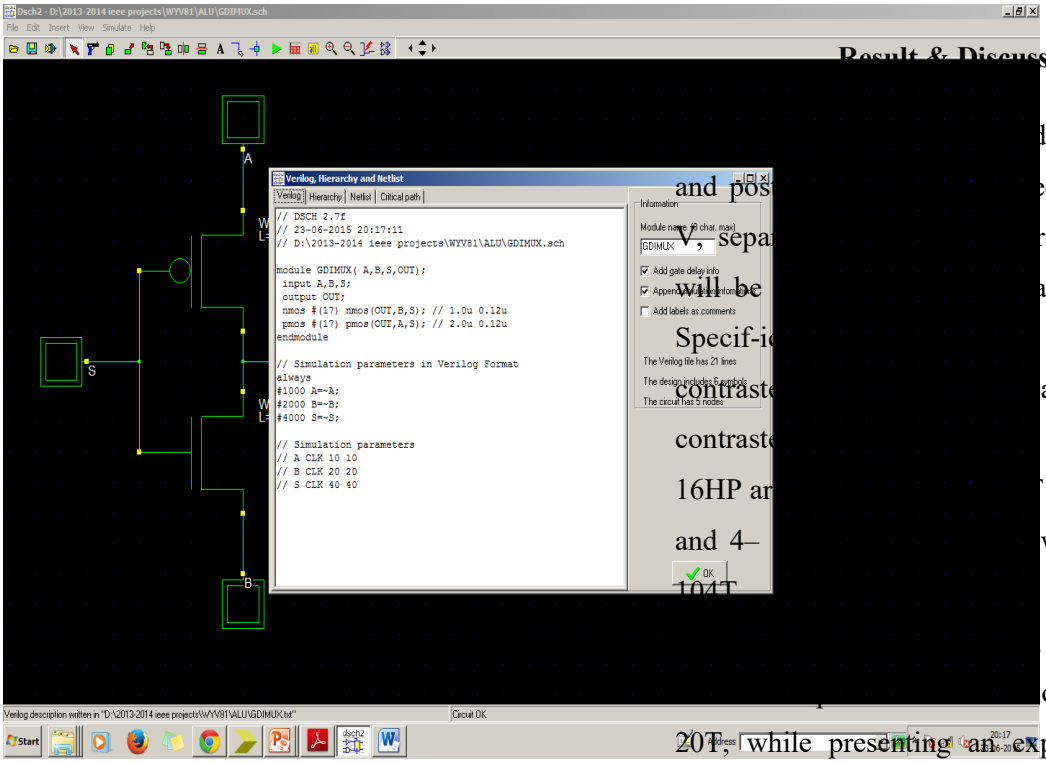

Simulate:

Result & Discussion

ds to power, PDP

ed in Tables III–

roposed de-signs

ditional partner.

2– 4HP are

and 2– 4HPI are

4– 16LP and 4–

lastly, 4– 16LPI

with rearranging

2– 4LP presents

on than CMOS

201, while presenting an expense of 26.7% higher postponement and 15.7% higher PDP.

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Then again, 2– 4HP beats CMOS 20T in all perspectives, diminishing force, deferral, and PDP by 8.2%, 4.3%, and 15.7%, separately. Both of our rearranging plans, 2– 4LPI and 2– 4HPI, beat CMOS 20T modifying in all viewpoints also. In particular, 2– 4LPI diminishes power, postponement, and PDP by 13.3%, 11%, and 25%,

TABLE III
POWER DISSIPATION RESULTS (IN NANOWATTS)

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	269	415	622	545	862	1287	1100	1768	2656	CMOS	641	1349	2050	1692	2751	4112	3395	5564	8310
2-4LP	246	386	576	495	799	1173.1	996	1594	2389	4-16LP	705	1258	1878	1577	2546	3816	3160	5140	7662
2-4HP	258	391	583	499	800	1185	1004	1618	2397	4-16HP	791	1270	1905	1588	2572	3847	3182	5198	7749
CMOS INV.	268	421	621	849	867	1290	1065	1767	2622	CMOS INV.	845	1330	2000	1698	2725	4096	3412	5562	8327
2-4LPI	242	381	567	488	778	1155	984	1571	2337	4-16LPI	788	1265	1888	1584	2566	3827	3178	5179	7724
2-4HPI	245	389	578	495	793	1175	988	1604	2377	4-16HPI	793	1271	1894	1592	2580	3841	3184	5209	7758

TABLE IV
PDP RESULTS (IN ELECTRONVOLTS)

2-4 DEC.	500 MHZ			1 GHZ			2 GHZ			4-16 DEC.	500 MHZ			1 GHZ			2 GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	176	127	128	357	264	265	720	541	543	CMOS	1125	817	836	2250	1666	1694	4532	3360	3425
2-4LP	203	149	155	406	306	315	821	617	636	4-16LP	995	739	750	1998	1478	1524	4094	2994	3061
2-4HP	153	115	120	306	235	244	620	475	494	4-16HP	963	698	702	1933	1413	1447	3873	2855	2854
CMOS INV	167	126	134	330	260	274	683	529	556	CMOS INV.	1326	897	886	2671	1844	1815	5367	3749	3680
2-4LPI	134	102	106	271	209	216	547	422	438	4-16LPI	1328	940	931	2669	1806	1887	5356	3846	3809
2-4HPI	133	102	105	269	208	213	542	420	430	4-16HPI	1203	849	839	2415	1723	1702	4844	3470	3436

TABLE V
2-4 DEC. PROPAGATION DELAY RESULTS (IN PICOSECONDS)

	0.8V	1.0V	1.2V	4-16 DEC.	0.8V	1.0V	1.2V
CMOS	105	49	33	CMOS	214	97	66
2-4LP	132	62	43	4-16LP	203	93	64
2-4HP	99	47	33	4-16HP	195	88	59
CMOS INV	100	48	34	CMOS INV.	252	108	71
2-4LPI	89	43	30	4-16LPI	270	119	79
2-4HPI	87	42	29	4-16HPI	243	107	71

CONCLUSION

This work presents a novel hybrid logic strategy for decoder circuit design that integrates Transmission Gate Logic (TGL), Dual Value Logic (DVL), and static CMOS. Utilizing this approach, we proposed four new 2-to-4 line decoder topologies—2-4LP, 2-4LPI, 2 4HP, and 2-4HPI—that offer improvements over conventional CMOS implementations by reducing transistor count and enhancing control delay performance. Building on this concept, we also introduced four new 4-to-16 line decoder designs—4 16LP, 4-16LPI, 4-16HP, and 4-16HPI. These architectures employ the newly designed 2-4 decoders as pre-decoding stages, followed by static CMOS post-decoders for robust output drive capability. Performance evaluations at the 32 nm technology node show that the proposed hybrid decoders consistently outperform standard CMOS counterparts in terms of power efficiency, delay, and Power-Delay Product (PDP). Among the designs:

- 2-4LP and 4-16LPI are best suited for area- and power-constrained applications.

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• 2-4LPI, 2-4HP, and 2-4HPI offer strong overall performance across metrics, making them suitable for a wide range of use cases. Given their low power dissipation and optimized transistor usage, the proposed decoders are well-suited for integration into large-scale digital systems, such as multiplexers, hierarchical decoders, and other combinational logic units with varying performance demands. Furthermore, these designs are compatible with both bulk CMOS and Silicon-On-Insulator (SOI) technologies. Their architectural efficiency also makes them suitable for standard cell library inclusion and RTL-level integration, enabling practical adoption in modern VLSI design flows.

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