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A BIDIRECTIONAL BATTERY CHARGER FOR A WIDE RANGE OF ELECTRIC VEHICLES

Dr .U. Narender
Department of Electrical & Electronics Engineering, Annamacharya Institute of Technology and Sciences, Hyderabad, Telangana, India
narendercmr1984@gmail.com

Mr. M. LALIYA
Department of Electrical & Electronics Engineering, Annamacharya Institute of Technology and Sciences, Hyderabad, Telangana, India
laliya18@@gmail.com

Y.ANUSHA
Research Scholar,
Department of Electrical & Electronics Engineering, Annamacharya Institute of Technology and Sciences, Hyderabad, Telangana, India
anushuyekula1208@gmail.com

Abstract

In this paper, a bidirectional buck-boost current-fed isolated DC-DC converter (B3CFIDC) is proposed to realize the bidirectional and buck/boost voltage conversion and accordingly extend the operating range. The basic modulation is proposed and the operation principle is analyzed in detail. Furthermore, the voltage conversion ratio as the functions of the duty cycle ratio of the buck unit and shoot through ratio of the H-bridge converter is derived. The control rule of the two controllable variables is determined based on minimizing the average inductor current. In addition, the optimal starting moment of active period of the buck unit in the switching cycle is determined based on minimizing the inductor current ripple. The detailed experimental results verify the correctness and feasibility of the proposed topology and modulation.

Index Terms -- Current-fed DC-DC converter, bidirectional boost-buck conversion, modulation optimization

I. INTRODUCTION

The bidirectional isolated DC-DC converter has attracted more and more attentions and has a wide potential application in the fields of electrical vehicle charger, solid state transformer, energy storage system because of the advantages of good soft-switching operation and wide voltage conversion range, and so on [1]-[6]. The bidirectional isolated DC-DC converter mainly includes the following several typical topologies. The first one is the dual active bridge (DAB) based DC-DC converter. In theory, this topology is capable of a wide voltage conversion and power transfer range and full soft-switching operation. However, its main shortcoming is the large current stress [7]-[10]. It results in a poor utilization rate of the current ratings of the power switches and other components and the system cost is high accordingly. The second one is the DAB DC-DC converter with the inductor-capacitor resonant tank as the energy storage component. This kind of topology possesses a better electromagnetic characteristic because of the quasi-sinusoidal operating current waveform and a better current ratio about 1.6 [11]-[16]. Due to these advantages relative to the DAB converter, the resonant-type DC-DC converter has been widely applied in the low-voltage and middle or small power systems.

However, in the case of the high voltage, the voltage across the resonant capacitor is very high. In addition, with the increasing of the power rating, the capacitance of the resonant capacitor will increase accordingly [11]. However, it is also very difficult to manufacture thus non-polar capacitor with so large capacitance and high voltage rating. The third one is the current-fed isolated DC-DC converter (CFIDC) [17]-[26]. The configuration difference from the inductor-based DAB DC-DC converter leads to a quite different operating principle between these two topologies. In theory, the CFIDC possesses a quasi-unity ratio between the peak and averaged values of the transformer current. It results in a best utilization rate of the power rating of the hardware as compared to other two kinds of topologies. However, from the schematic of the CFIDC, it is essentially equivalent a standard boost DC-DC converter if neglecting the transformer current polarity reversion process. It means it can realize only the boost conversion. However, in many actual applications, i.e. the battery or the super capacitors charging/discharging systems, the wide variation of the terminal voltage of the energy storage components requires that the charging/discharging system is capable of wide voltage conversion range. It is obvious that the feature of only boost conversion is not well suitable for thus application. In order to preserve the advantages of quasi-unity current ratio of the CFIDC and extend its voltage conversion range, thus possessing a wide application fields, in this paper, a bidirectional boost-buck CFIDC is proposed. Furthermore, the control rule of the duty ratio cycle of the buck unit and the shoot through period of the H-bridge converter is determined based on minimizing the average inductor current. Additionally, by limiting the inductor current ripple, the ideal duration of the rising edge of the power switch of the buck unit with respect to the beginning of the switching cycle is established. To highlight the benefits of the suggested topology, it is contrasted with a number of well-known DC-DC converters.

II. BIDIRECTIONAL DC-DC CONVERTER

Switching power supplies in the tens of kilowatt power range have been slowly replacing traditional silicon controlled rectifier (SCR) based topologies over the past several decades. The advantages and disadvantages are well known. High frequency operation of switching power supplies enables magnetic components to be reduced in size and weight and allows faster

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response times to line and load perturbations. The principle disadvantage is that the demands placed on switching devices tend to make high power switching power supplies less reliable than their SCR based counterpart.

Numerous power circuit topologies are currently being deployed for high-power switch mode applications. The most common configurations consist of three power conversion stages:

- An AC to DC converter which converts the 3-phase incoming mains to a DC voltage.
- A DC to AC inverter or converter which converts the voltage on the DC bus to a high-frequency AC voltage.
- A secondary AC to DC converter which converts the high-frequency AC voltage to DC voltage.

The two AC to DC converters are very similar in function except for the operating frequencies; the converters consist primarily of rectifiers, low pass filters, and snubbers. The snubbers limit switching transient voltages and absorb energy stored from parasitic components. The second stage, the DC to AC converter, generates a high-frequency voltage which drives a transformer at a frequency generally at 20 kHz or above. The transformer is required for ohmic isolation and production of an output voltage as determined by the transformer turns ratio. The DC to AC converter is the most complex stage and there are numerous power processing topologies presently in production.

Most high-power DC to AC converters utilize a H-bridge configuration, four power devices, for exciting the high-frequency transformer. The H-bridge is controlled with pulse width modulated (PWM) or with other modulation strategies to produce a voltage of limited pulse width or amplitude. Modulation of the H-bridge produces a controllable output voltage.

DC to AC converter topologies fall into three groups: hard-switched converters, soft-switched converters, and resonant converters. The primary difference between the topologies is the switching device's load line during the commutation period (switching transition). It is during the commutation period where power devices dissipate the most power.

Hard-switched converters allow the power devices and/or snubbers to absorb commutation energy. Soft-switched converters have additional passive circuitry to shape power waveforms to reduce losses during the commutation period. The advantage of reduced commutation losses is offset with increased circuitry complexity, additional on-state losses (due to waveform modification), and sensitivity to loading conditions. Resonant power converters have highly tuned tank circuits which cause either device voltage or current to appear sinusoidal. The advantages and disadvantages are similar to soft-switched converters. Resonant power converters are second-order and timing is more critical than soft-switched converters.

Hard-switched, soft-switched, and resonant converters are usually designed to operate from a DC voltage source and are commonly referred to as voltage-fed converters. Characteristically, voltage-fed converters are prone to shoot through problems which can occur when one device fails to turn off before the other series connected device turns on. While protective circuitry can be designed to minimize catastrophic problems, generally, such protective circuitry must be effective to detect shoot though problems in one to two microseconds. Variation of device parameters and abnormal modulation of voltage-fed converters can cause half-cycle voltage imbalance which can result in transformer core saturation. Protective circuitry must also have a response to detect these conditions before damage can occur in the power semiconductors.

Current-fed power converters, the electrical dual of voltage-fed converters, is still another, but less known and used, power circuit alternative for power conversion. The advantage of these power converters over their voltage-fed counterpart is that shoot through and half cycle symmetry cannot cause device failure or core saturation. This is characteristic of SCR based converters and one of the main reasons why current-fed converters tend to be more robust. The main disadvantage of current-fed converters is that a fourth power conversion stage is required to convert the DC bus voltage to a DC current. While the added stage results in additional complexity and losses, the power conversion stages can be made to work more efficiently. Current-fed power converter topologies are implemented less than voltage-fed converters primarily because of cost.

This article describes the differences between voltage-fed and current-fed converters and the sensitivities to conditions causing power semiconductor stress. Issues for implementing the fourth power conversion stage, the voltage to current converter, are also discussed.

The proposed bidirectional buck-boost current-fed isolated DC-DC converter (B3CFIDC) is shown in Fig. 1, including one bridge arm composed of the switches S11 and S12, inductor L, H-bridge converter (HB1), H-bridge converter (HB2) and a high frequency isolation transformer (HFT). Llk and n are the leakage inductor and winding ratio of HFT, respectively. L, HB1, HB2 and HFT constitute a standard current-fed isolated DC-DC converter. From [19], it can only achieve boost operation when power is transferred from U1 to U2 and only achieve buck operation in reverse direction. For the proposed converter, when power is transferred from U1 to U2 (forward mode), S12 is turned off and its equivalent circuit is shown in Fig. 2(a).

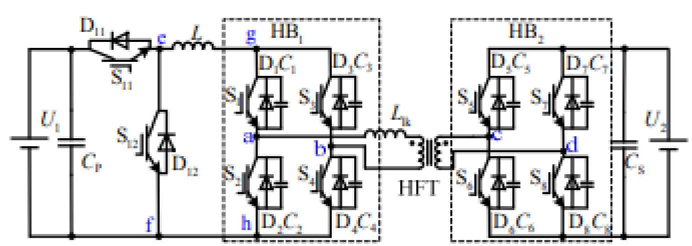

Fig. 1 Schematic of proposed B3CFIDC

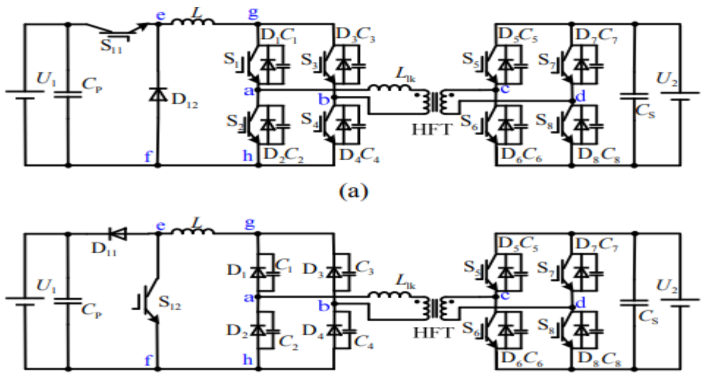

Fig. 2 Equivalent circuits of proposed topology in two transfer directions (a) From U1 to U2 (forward mode), (b) from U2 to U1 (reverse mode).

Besides the normal boost operation, it can achieve the buck operation by controlling the duty cycle d11 of S11 in forward mode. When power is transferred in reverse direction, switch S11 is turned off and its equivalent circuit is shown in Fig. 2(b). The proposed converter can achieve the boost operation by controlling the duty cycle d12 of S12 in reverse mode. According to the above analysis, by adding switches S11 and S12, the proposed topology can realize a bidirectional power transfer and buck-boost operation. In this section, the operating principle of proposed topology is analyzed to lay the foundation for the subsequent modulation strategy and optimization scheme. Considering that the operating process of the proposed topology in two power transmission directions is dual, in order to save page space, this paper only analyses the working process of forward mode. From [19] and Fig. 2(a), in forward mode, it needs to control the short through period of HB1 to achieve the boost operation. At the same time, the diagonal switch pairs of HB2 need to be turned on for a short time in each switch cycle to control the transformer current actively. So that the transformer current can reach the inductor current actively before the converter becomes power transfer state, so as to avoid the sudden change of transformer current and the voltage spike caused by the current mutation. The turn-on time ratio of the diagonal switch pairs of HB2 is defined as ds. In addition, there is another controllable variable, which is the duty cycle d11 of S11.

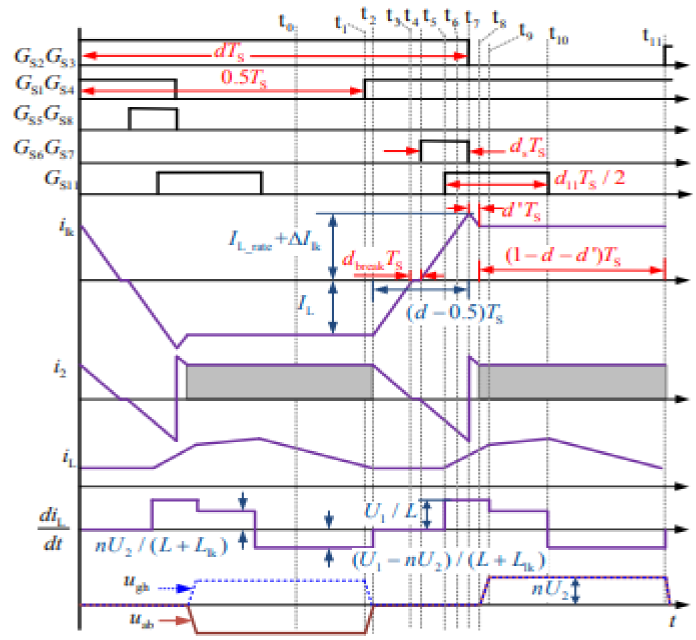

Fig. 3 General modulation waveforms of proposed converter

A general case of the modulation waveforms considering the above situation is shown in Fig. 3 Fig. 4 is the corresponding equivalent circuits of the proposed converter during different intervals in Fig. 4. In the following analysis, assuming that the energy storage inductor L is large enough to maintain a constant average current IL through it and the current ripple is small enough to be ignored. The exaggerated waveform of instantaneous current of energy storage inductor (denoted as iL) is also shown in Fig. 4 for the convenience of observation. The control signals of S2, S3 of HB1 lag those of S1, S4 in a half switching cycle. The simultaneous conduction period of diagonal power switches of HB1 is defined as dTS, and then the short through period of HB1 is

$$t_{\text{shoot}} = (d - 0.5)T_S \qquad (1)$$

Where

T_S is the switching cycle. The operating process of the proposed converter in each interval of the operating waveforms shown in Fig. 4 is analyzed as follows. [t0, t1): In this interval, S11 keeps off state and iL flows through D12. S2 and S3 of HB1 are under on state and the secondary current of HFT inputs to U2 through D6 and D7. U1 does not output power, the inductor L can be seen as a current source transferring the power from the primary side to the secondary side of HFT. More accurately, iL decreases gradually under the action of nU2. [t1, t2): At t1, S1 and S4 are turned on, and C1 and C4 begin to discharge. The voltage uab rises from -U2 to zero in a very short time. When uab reaches zero at t2, the transformer current rises under the action of U2, iL and ilk are no longer equal to each other. From KCL law, the current flowing through S1-4 begins to increase from zero. [t2, t3): At t2, S1-4 is all turned on, the two bridge arms of HB1 are both under shoot-through state.

iL flows through D12 and the two bridge arms of HB1. iL remains constant because of zero voltage drop on L. The voltage across Llk is in Fig. 4 It begins to rise under the action of U2. Starting from this interval, the currents through the power switches of HB2 are.

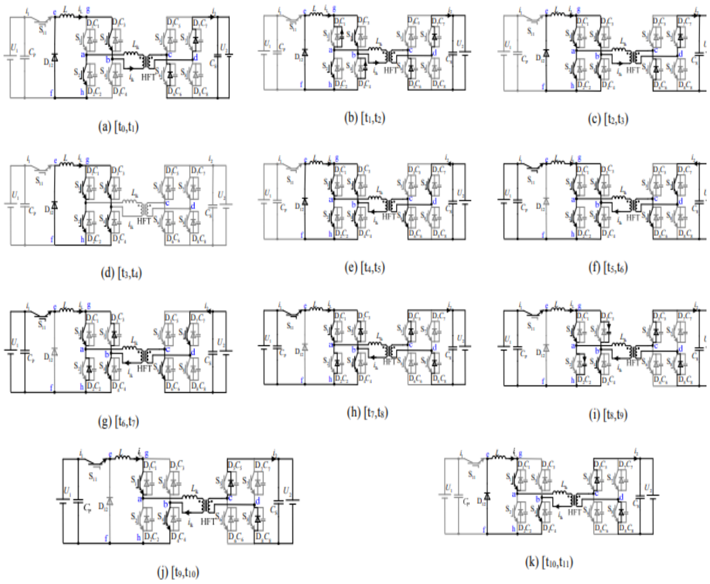

Fig. 4 Equivalent circuits of different intervals

$$u_{lk} = u_{ab} - nU_2 \approx -nU_2 \tag{2}$$

So i_{lk} can be approximately expressed as

$$i_{lk} = -I_L + nU_2(t - t_2) / L_{lk} \tag{3}$$

The currents through S1 and S4 begin to = =2 D7 D6 lk i i i ni rise from zero and the current through S2 and S3 begin to decrease from IL. The instantaneous current of each switch of HB1 can be expressed as

$$i_{S2} = i_{S3} = I_L - nU_2(t - t_2) / (2L_{lk}) \tag{4}$$

$$i_{S1} = i_{S4} = nU_2(t - t_2) / (2L_{lk}) \tag{5}$$

[t3, t4): At t3, ilk reaches zero. The currents through S1 and S4 rise to IL/2, and the currents through S2 and S3 decrease to IL/2. Because all of the power switches of HB2 are under off state, ilk and the currents through S1-4 remain constant. D6 and D7 of HB2 are turned off softly because ilk reached zero. This period is defined as break S d T, shown in Fig. 3. [t4, t5): At t4, S6 and S7 are turned on, U2 is applied to the 0, ilk begins to raise=secondary side of HFT. Because abu from zero under the action of U2. It leads that the currents through S1 and S4 begin to rise from IL/2 and the current through S2 and S3 begin to decrease from IL/2. Starting from this interval,

$$i_2 = i_{S7} = i_{S6} = ni_{lk}$$

[t5, t6): At t5, S11 is turned on, then U1 is applied to the 0, iL is expressed as=inductor L. Because uab=0 iL is expressed as

$$i_L = i_L(t_5) + (U_1 - u_{ab})(t - t_5) / L = i_L(t_5) + U_1(t - t_5) / L \tag{6}$$

Because L is much larger than Llk, the rising rate of Li is much less than the raising rates of lk i. The energy is stored in L from U1.

[t6, t7): At t6, lk i rises to IL and the currents through S1 and S4 also rise to IL, and the currents through S2 and S3 decrease to zero. The current lk i has two flowing paths: the first one is from S1 to D3, and the other one is from D2 to S4. The currents through HB1 are expressed as

$$i_{D2} = i_{D3} = 0.5(i_{lk} - I_L) \tag{7}$$

$$i_{S1} = i_{S4} = 0.5I_L + 0.5(i_{lk} - I_L) = 0.5i_{lk} \tag{8}$$

[t7, t8): At t7, S2, S3, S6 and S7 are turned off. S2 and S3 are under zero-current switching (ZCS) because no current flow and ilk will– ≈ 0, lk 2 u nU =through them. Because ab u decreases gradually. It means lk i reaches its maximum at t= t7, which is defined as lk_max i. In order to ensure there is no voltage spike in the entire power range, lk_max i should be designed based on the rated inductor current L_rate I and I is considered. So lk_max i can beΔa current margin lk expressed as

$$i_{lk\_max} = I_{L\_rate} + \Delta I_{lk} \tag{9}$$

Because lk i begins to decrease, the currents through S1, S4, D2 and D3 also begin to decrease. Therefore, the current stress of each power switch can be obtained from (7) - (9).

$$i_{D1\text{-}4} = i_{S1\text{-}4} = I_{L\_rate} + 0.5\Delta I_{lk} \tag{10}$$

And the secondary transformer current flows from D5 to U2 to D8. It means the converter operates at the normal power transfer state. Furthermore, the period of [t7, t8) is

$$d'T_S = (I_{L\_rate} + \Delta I_{lk} - I_L)L_{lk} / nU_2 \tag{11}$$

$$i_L = i_L(t_9) + (U_1 - nU_2)(t - t_9) / (L + L_{lk}) \tag{12}$$

[t10, t11): At t10, S11 is turned off and iL flows through D12. .+iL begins to decreases with the rate of 2 lk ( )/( ) nU L L Next, the relationship between the controllable variables d11, d, ds, the voltage conversion ratio k=nU2/U1, and IL is analyzed. The average voltage between point e and f shown in Fig. 2 is defined as Uef and the average voltage between point g and h shown in Fig. 3 is defined as Ugh. Obviously, the waveform of the instantaneous voltage between g and h can be obtained by rectifying the waveform of uab shown in Fig. 4, so Ugh can be obtained by calculating the average value of uab in a half switching cycle. The two average voltages can be expressed as

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$$U_{ef} = d_{11}U_1 \quad (13)$$

$$U_{gh} = 2(1-d-d')nU_2 \quad (14)$$

The volt-second product of L at the steady state is zero in the half switching cycle. It means

$$U_{ef} = U_{gh} \quad (15)$$

Thus, the relationship between the voltage conversion ratio and the controllable variables can be obtained as

$$k = \frac{nU_2}{U_1} = \frac{d_{11}}{2(1-d-d')} \quad (16)$$

By substituting (11) into (16), k is expressed as

$$k = \frac{d_{11}}{2\left[1-d-L_{lk}\left(I_{L\_rate}+\Delta I_{lk}-I_L\right)/\left(nU_2T_S\right)\right]} \quad (17)$$

From (16), because of d, the converter>> 0.5 and d ' 0 can achieve the boost and buck operation by varying d11 and d cooperatively.

III. CONTROL STRATEGIES

According to the above analysis, the voltage conversion ratio can be tuned by varying the controllable variables d11 and d. For a certain voltage conversion ratio, d11 and d have infinite combinations. So it is necessary to introduce some appropriate constraint to obtain the exact relationship between d11, d and k. In addition, the variation of the position of S11 under on state in the entire control cycle does not affect the voltage conversion ratio; however, it will affect the current ripple of inductor. In this section, the position of S11 under on state relative to the control signal of HB1 will be obtained by minimizing the current ripple of inductor.

A. Control Rule of ds, d11 and d to Reduce Average Inductor Current

Following is an analysis of the design principle of the turn-on time ratio ds of the diagonal switch pairs of HB2. The function of ds is to make the transformer current to rise actively by adding the voltage 2 nU at the leakage inductor Llk, so that the voltage spike can be eliminate. Fig. 2.6 shows that during the turn-on period of the diagonal switch pairs of HB2, U1 does not output power and the power flows to Llk from U2, which can be equivalent to the reactive power. Therefore, this period (dsTS) should be as short as possible to avoid occupying too much effective power transfer time. The expression of primary transformer current is

$$i_{lk} = nU_2t / L_{lk} \quad (18)$$

$$d_s = \frac{L_{lk}i_{lk\_max}}{nU_2} = \frac{L_{lk}}{nU_2}\left(I_{L\_rate}+\Delta I_{lk}\right) \quad (19)$$

Therefore, when the required ilk_max and U2 remain unchanged, ds is mainly proportional to Llk. The smaller Llk is, the smaller ds will be. In the actual system, it is necessary to consider the manufacturing process of the transformer, in order to avoid its design value too small to be realized in the actual production process. In order to simplify the control complexity, in the entire power range and voltage conversion range, ds is always designed according to (19) and remain unchanged in this paper. Next, the control principle of d11 and d are analyzed. According to the principle of the converter, the relationship between the average input current I1 and IL is

$$I_1 = d_{11}I_L \quad (20)$$

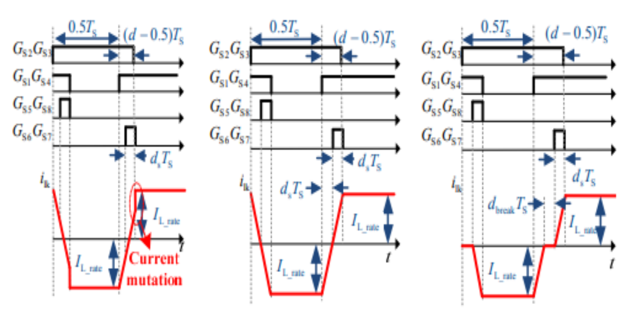
From the waveform of the output current i2 shown in Fig. 4, the effective part of i2 is the area of the shadow part. The average value of i2 can be expressed as

$$I_2 = 2I_L(1-d-d') \quad (21)$$

From the above two equations, under the premise of transferring the same rated power, the larger d11 is, the smaller IL will be. Reducing IL is beneficial to reduce the loss of power devices, inductors L and HFT. Therefore, the larger d11 and the smaller d should be chosen as far as possible. Furthermore, from (16), in order to obtain the same voltage conversion ratio, if d11 is increased, d should be reduced accordingly. Therefore, for a given k, d11 should be as large as possible while d should be as small as possible to reduce IL. Considering that k is proportional to d11 and inversely proportional to d, when the converter is under buck operation, d is taken as the minimum. When the converter is under boost operation, d11 is taken as 1 and various voltage conversion ratios can be achieved by adjusting d.

The principle of determining the minimum of d is analyzed below. According to the above analysis, in order to eliminate the voltage spike, HB2 is required to provide the voltage actively for a short time in each half switching cycle so that the primary transformer current can rise as soon as possible and exceed IL. In order to obtain the fastest variation rate of the primary transformer current, during the period when HB2 provides the reverse voltage, the AC-side output voltage of HB1 uab should be equal to zero. Therefore, the short-through period of HB1 should be greater than or equal to twice the period of HB2 providing reverse voltage. So the constraint of d is

$$(d-0.5) \geq 2d_s \quad (22)$$



(a) $(d-0.5)<2d_s$ (b) $(d-0.5)=2d_s$ (c) $(d-0.5)>2d_s$

Fig. 5 Waveforms of polarity conversion process of the primary transformer current under different conditions

B. Pulse-Width Modulation

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PWM is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load. Along with maximum power point tracking (MPPT), it is one of the primary methods of reducing the output of solar panels to that which can be utilized by a battery. PWM is particularly suited for running inertial loads such as motors, which are not as easily affected by this discrete switching, because their inertia causes them to react slowly. The PWM switching frequency has to be high enough not to affect the load, which is to say that the resultant waveform perceived by the load must be as smooth as possible.

The rate (or frequency) at which the power supply must switch can vary greatly depending on load and application. For example, switching has to be done several times a minute in an electric stove; 100 or 120 Hz (double of the utility frequency) in a lamp dimmer; between a few kilohertz (kHz) and tens of kHz for a motor drive; and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies. The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle. PWM has also been used in certain communication systems where its duty cycle has been used to convey information over a communications channel.

VI. SIMULATION RESULTS

MATLAB is an interactive system whose basic data element is an array that does not require dimensioning. This allows solving many technical computing problems, especially those with matrix and vector formulations, in a fraction of the time it would take to write a program in a scalar non-interactive language such as C or FORTRAN.

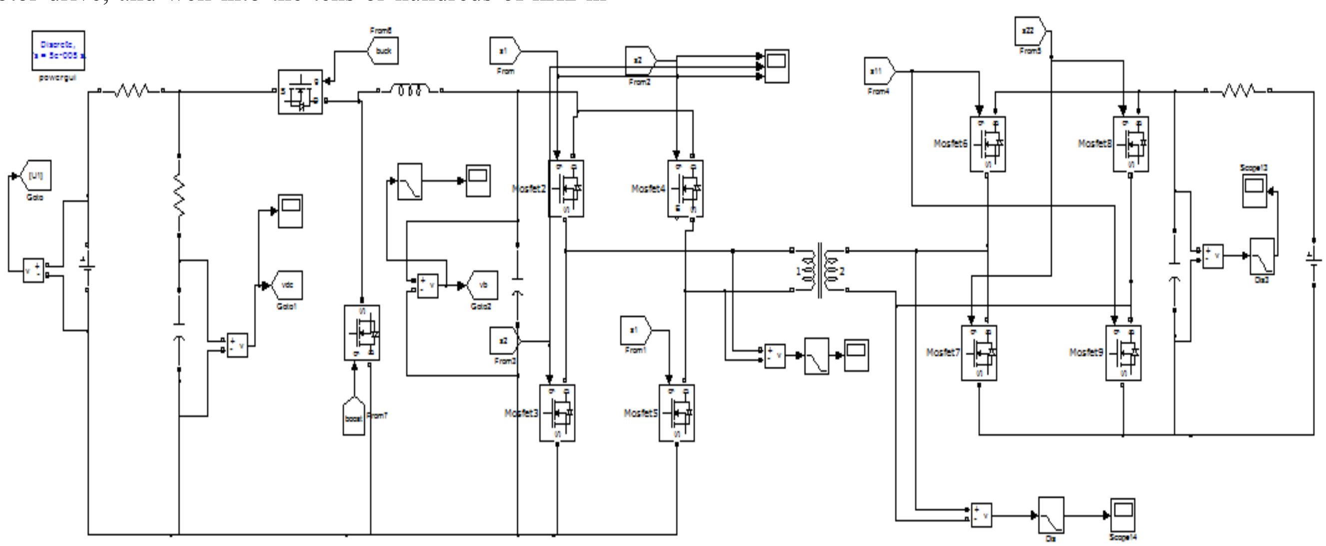

Fig.6 Simulation circuit

The recommended circuit was developed using input dc sources, input power electronic switches (IGBT, Thyristors), and Matlab/Simulink. In Figure 6, it is shown.

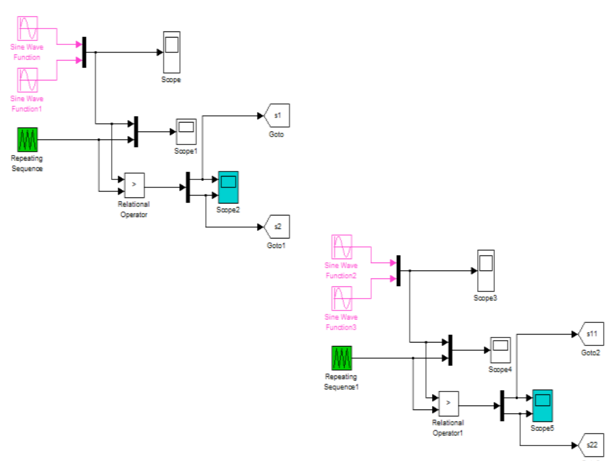

Fig. 7 Control circuit

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The suggested model sends the input from a dc source block to the first half bridge (HBT) after it has been separated with a transformer using Simulink source and signal blocks in Matlab.

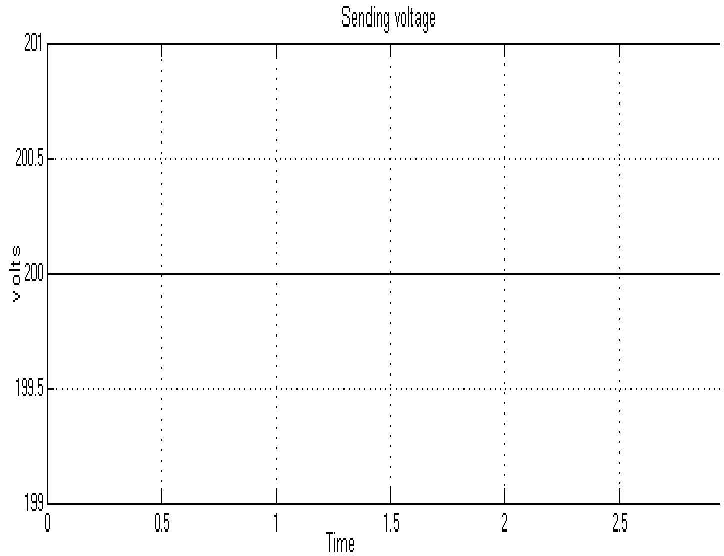


Fig.8 Sending input voltage

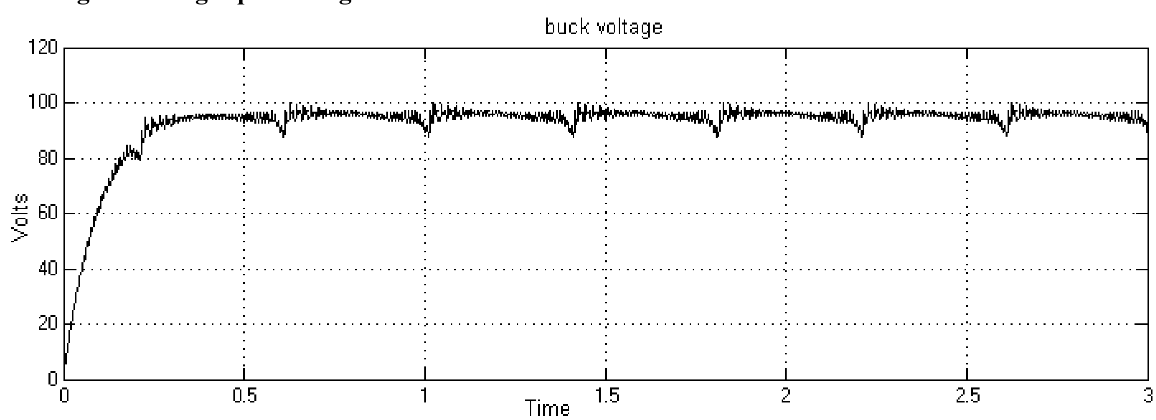
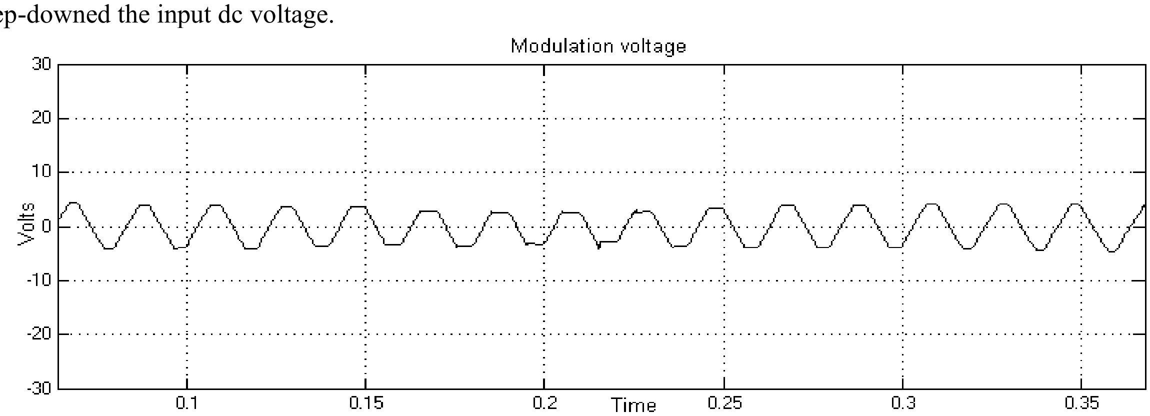
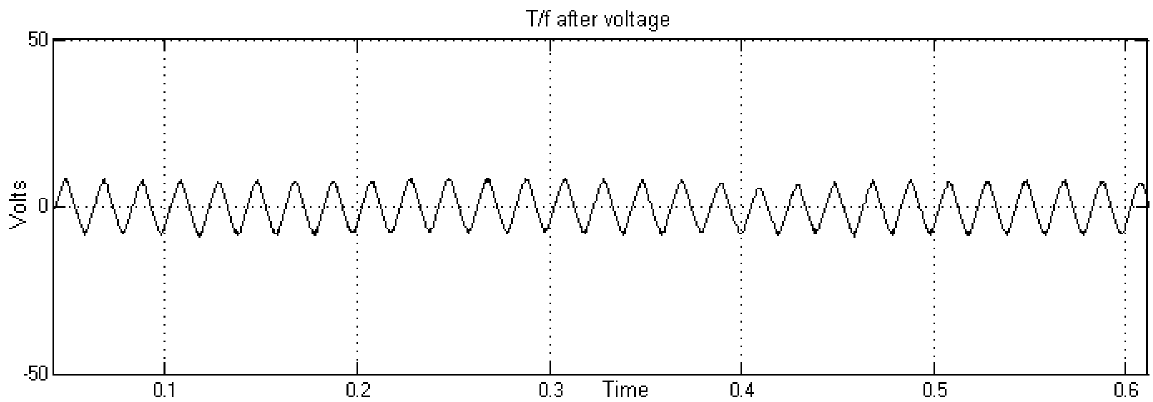


Fig. 9 Step up voltage

As seen in figures 8 and 9, the input supply and buck-boost converter step-downed the input dc voltage.



(a)



(b)

Figure 10 (a) and (b) above depicts the transformer's primary side and secondary side voltages.

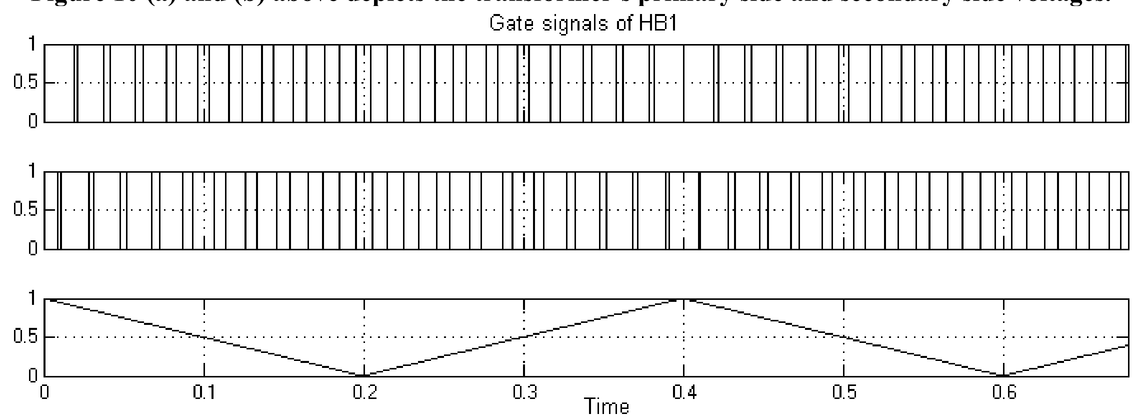


Fig. 11 Gate signals

The pulse signals of the suggested HBT converters are shown in the figures above. To generate an output signal, HBT uses two hall bridge operations.

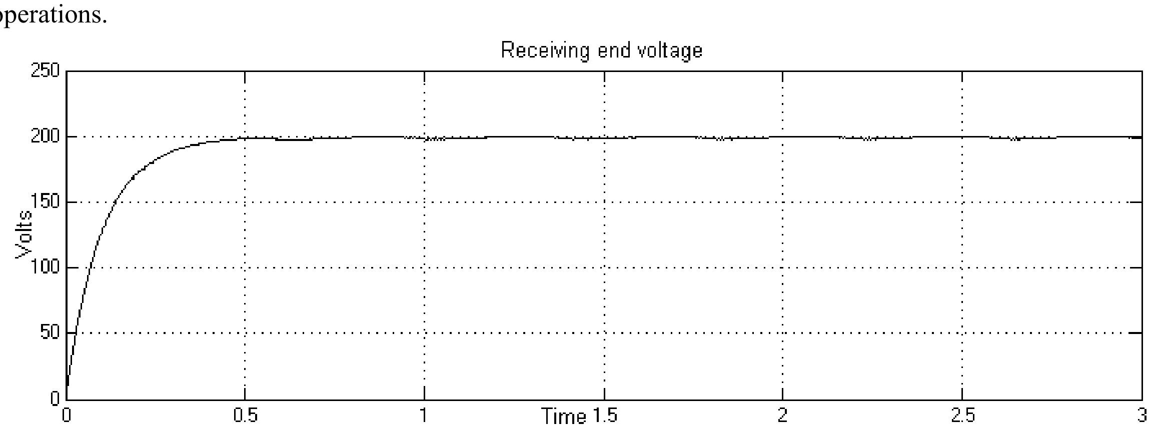


Fig. 12 Receiving end voltage

Furthermore, in order to further verify the advantages of the proposed topology in terms of the voltage conversion range, current stress and cost, it is compared with the typical voltage-type dual active bridge (DAB) based DC-DC converter, LC series resonant DC-DC converter and the boost current-fed isolated DC-DC converter. The corresponding comparative data are shown in Table IV. According to the existing literature, the ratio of peak to average current in DAB converter is about 2, the ratio of peak to average current in LC resonant converter is 1.6, and the ratio of peak to average current in current-fed converter is about 1.

TABLE IV
Data of Several Bidirectional Dc-Dc Converters

	DAB	Resonant	Current-fed	Proposed
Voltage conv. range	Buck-boost, wide	Buck-boost, wide	Boost, narrow	Buck-boost, wide
Current stress ratio	2	1.6	1	1
Number of switch	8	8	8	10
Number of equivalent switch	16	12.8	8	10
Cost ratio of switch	1.6	1.28	0.8	1

The number of equivalent power switches is defined as the product of the current stress ratio and the actual number of switching devices. Under the same transfer power, in order to simplify the comparison, the number of equivalent power switches and cost ratio are calculated according to the approximately proportional relationship of the current rating. From Table IV, at the same power, the number of equivalent power switches of the proposed topology is reduced by 50% and 28% compared with DAB and LC resonant DC-DC converters, respectively. The voltage conversion range is significantly extended compared with the boost current-fed DC-DC converter. Therefore, the proposed topology has excellent comprehensive performance.

- The dual active bridge converter connects a battery energy storage system to a DC bus so to provide a high level of reliability and resilience to grid disturbances.
- In particular, the proposed converter ensures a stable DC bus voltage when the micro grid is operated in islanded mode.
- **Vehicles:** In the case of vehicles, the main DC/DC converter changes power from the onboard high voltage battery into lower DC voltages used to power lights, wipers, and window controls.
- **Smart lighting:** Several lighting applications require LED backlight driver solutions that possess high efficiency, direct current control, voltage protection, PWM-based control, and simple design.

V CONCLUSION & FUTURE SCOPE

Bidirectional boost and buck operations are made possible by the proposed bidirectional boost-buck current-fed isolated DC-DC converter. A low average inductor current and current ripple are achieved with the suggested modulation approach and the cooperative control method of shoot-through duty cycle and buck duty cycle, and the voltage spike is prevented over the full operating range. The comparison between the proposed topology and several typical DC-DC converters shows that the proposed topology has lower cost ratio under the premise of realizing the bidirectional boost and buck operation. The cost of the proposed topology is 40% lower than that of the DAB DC-DC converter and 22% lower than that of the resonant converter, respectively. The proposed topology has better practical value.

Future Scope

- The most common criteria that need to be met during the design of DC/DC converters include maximizing performance and enhancing power density while reducing the overall cost.
- Some key applications where DC/DC converters are employed extensively include renewable energy integration, medical devices, vehicles, smart lighting, and other small-scale electronic appliances.

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AUTHOR PROFILE

Dr. U. Narender has Associate Professor in ELECTRICAL AND ELECTRONICS ENGINEERING at ANNAMACHARYA INSTITUTE OF TECHNOLOGY& SCIENCES, Hyderabad, India .Has 15 years of teaching experience in engineering collegesHe has received his Ph.D. in Electrical Engineering From JJTU University in 2021 and M.Tech in power Electronics from CMR college of Engineering & Technology in 2010 and B.Tech in Electrical and Electronics Engineering from Sindhura Institute of Engineering & Technology in 2006.

Areas of interests are WOT (WEB of things), Artificial Intelligence, Cloud computing, Power Electronics, Control Systems, power systems and Electrical machines.

EMAIL ID: narendercmr1984@gmail.com
narender0866@yahoo.co.in

M. LALIYA has Associate Professor in ELECTRICAL AND ELECTRONICS ENGINEERING at ANNAMACHARYA INSTITUTE OF TECHNOLOGY& SCIENCES, Hyderabad, India .Has 14 years of teaching experience in engineering colleges He has M.Tech in power Electronics from KNR college of Engineering & Technology in 2016 and B.Tech in Electrical and Electronics Engineering from NETAJI Institute of Engineering & Technology in 2010.

Areas of interests are WOT (WEB of things), Artificial Intelligence, Cloud computing, Power Electronics, Control Systems, power systems and Electrical machines.

EMAIL ID: laliya18@gmail.com

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SCHOLAR DETAILS:

M. ANUSHA. Has 1 years of MANUFACTURING experience. Presently he is working as ENGINEER TRAINE in FOXCONN INTERCONNECT TECHNOLOGY . He Completed B-Tech in SREE DATTHA INSTITUTE OF ENGINEERING AND SCIENCE .His Interested Subjects Are Power Electronics, Electrical Traction, Electrical Drives, Control Systems.
EMAILID: anushuyekula1208@gmail.com.