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Design of Generic Vedic ALU Using Reversible Logic

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ABSTRACT

In today's high-performance computing landscape, real-time applications demand rapid processing units with optimal power efficiency. The Arithmetic Logic Unit (ALU) and Multiply-Accumulate (MAC) unit are fundamental to digital signal processing (DSP) and processor architectures. Among these, the multiplier is the most critical and computationally expensive component. This paper proposes the design of a Generic Vedic ALU based on the Urdhva Tiryakbhyam sutra of Vedic Mathematics, incorporating reversible logic gates for energy efficiency. The proposed 16-bit Vedic multiplier generates all partial products in a single step, significantly reducing propagation delay compared to conventional array multipliers. The design is implemented using Verilog HDL and synthesized on the Xilinx Vivado platform targeting FPGA. Simulation results demonstrate superior performance in terms of area utilization (LUT: 476, 0.35%), propagation delay (25.130 ns), and power consumption. The architecture is suitable for applications in DSP, image processing, biomedical signal processing, and cryptographic systems.

Keywords: *Vedic multiplier, Urdhva Tiryakbhyam, Reversible Logic, Array Multiplier, Verilog HDL, FPGA, ALU, Low Power VLSI Design.*

I. Introduction

The rapid growth in digital processing requirements has led to increasing demand for high-speed, lowpower arithmetic circuits. The Arithmetic Logic Unit (ALU) lies at the heart of every microprocessor, digital signal processor (DSP), and application-specific integrated circuit (ASIC). Of all arithmetic operations, multiplication is the most resource-intensive, consuming the majority of execution time in applications such as FIR/IIR filtering, Fast Fourier Transforms (FFT), Discrete Cosine Transforms (DCT), and image processing.

Conventional multiplier architectures such as array multipliers and Booth multipliers suffer from high propagation delay, large hardware area, and significant power dissipation due to the sequential nature of carry propagation.

These shortcomings are addressed by Vedic Mathematics, an ancient Indian mathematical system rediscovered by Swami Bharati Krishna Tirthaji Maharaj, which offers 16 sutras (aphorisms) for rapid mathematical computation.

The Urdhva Tiryakbhyam (UT) sutra, translating to 'Vertically and Crosswise', provides a generalized multiplication algorithm that computes all partial products simultaneously, thereby enabling parallel processing and significantly reducing latency. This paper presents a 16-bit Generic Vedic ALU based on this sutra and enhanced with reversible logic gates, which eliminate information loss and reduce heat dissipation — a key concern in nanoscale VLSI design.

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Literature Review

Several research works have explored Vedic multiplier architectures and their implementations:

Prabhu et al. [1] proposed a delay-efficient Vedic multiplier utilizing the Nikhilam and Urdhva Tiryakbhyam sutras, demonstrating reduced propagation delay compared to Modified Booth multipliers. Ram et al. [2] designed an area-efficient modified Vedic multiplier coded in Verilog HDL and synthesized using Xilinx, showing improvements over array multipliers in delay, memory, and power. Thapliyal and Arabnia [3] introduced a time-area-power efficient Vedic multiplier and square architecture for FPGA, proving faster operation than both array and Booth multipliers. Ramalatha et al. [4] designed a high-speed, energy-efficient ALU using Vedic multiplication techniques, employing the Urdhva Tiryagbhyam sutra in a co-processor to reduce execution time and area.

Tiwari et al. [5] proposed a low-power, high-speed multiplier based on Vedic Mathematics for SoC applications. Bansal et al. [6] reviewed various high-speed Vedic multiplier designs and concluded that compressor-based Vedic multipliers yield the best trade-offs in speed and area. Panda et al. [7] implemented a novel 8-bit Vedic multiplier using the Urdhva Tiryakbhyam sutra with carry-skip addition in VHDL, achieving minimum delay. Kerur et al. [8] implemented Vedic multipliers in image compression using the DCT algorithm, demonstrating significant computational speed improvements. The literature consistently highlights the advantages of Vedic multipliers over conventional architectures, particularly in terms of speed and area optimization.

II. Existing Method: Array Multiplier

The Array Multiplier (AM) is a conventional hardware multiplier based on the 'add and shift' algorithm. It computes the multiplication of two n-bit numbers through three sequential stages: Partial Product Generation (PPG), Partial Product Reduction (PPR), and Final Addition.

In PPG, an array of AND gates computes all n^2 partial products. These are then reduced using Half Adders (HA) and Full Adders (FA) arranged in a grid. For an n×n multiplier, n^2 AND gates, n×(n-2) Full Adders, and n Half Adders are required. For a 4×4 multiplier, this requires 16 AND gates, 4 HAs, and 8 FAs, totaling 12 adders. The 8×8 array multiplier requires significantly more hardware and exhibits high propagation delay due to carry ripple.

Disadvantages of Array Multiplier

- High propagation delay due to carry rippling through adder stages
- Large area requirements as bit width increases
- High hardware complexity with increasing number of computations
- High dynamic power consumption due to switching activity
- Reduced overall system performance in high-speed applications

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III. Proposed Method: Vedic Multiplier

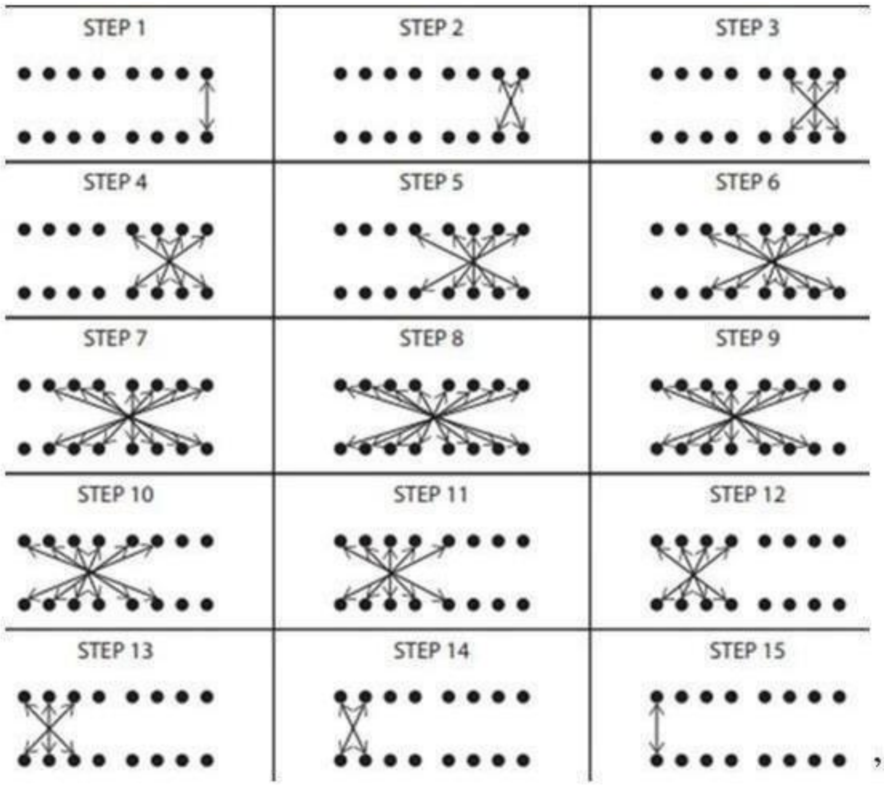

Fig 1: Proposed Vedic ALU

A. Vedic Mathematics and UT Sutra

Vedic Mathematics, attributed to Swami Bharati Krishna Tirtha (1884–1960), consists of 16 sutras and 13 sub-sutras applicable to various branches of mathematics. Among these, the Urdhva Tiryakbhyam (UT) sutra is the most efficient for binary multiplication. The term 'Urdhva' means vertical and 'Tiryakbhyam' means crosswise, describing the manner in which digit pairs are multiplied and accumulated.

The UT algorithm generates all partial products and their sums in a single step, unlike conventional methods that require sequential carry propagation. This parallel partial product generation significantly reduces computation latency. The algorithm is universally applicable to all n×n bit multiplications and scales gracefully with increasing operand widths, with gate delay and area growing much more slowly than in array multipliers.

B. 16-bit Vedic Multiplier Architecture

The proposed design implements a 16-bit Vedic multiplier for inputs X[15:0] and Y[15:0], producing a 32bit product P[31:0]. The architecture decomposes 16×16-bit multiplication into four 8×8-bit submultiplications, each further decomposed into 4×4-bit Vedic modules.

The key steps of the UT multiplication algorithm for two n-bit numbers are as follows: (1) multiply vertically the rightmost bit pair; (2) crosswise multiply and add with the carry from step 1; (3) continue shifting the crosswise multiplication window leftward, accumulating partial products column-wise; (4) the least significant bit of each column sum becomes a result bit, while the remaining bits form the carry to the next column.

Internal carry bits c[1] to c[89] are generated during computation. Addition of higher-order inputs is performed using compressor architectures, which map multiple inputs to a reduced number of outputs more

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efficiently than chains of full adders. This compressor-based approach enhances speed and reduces area compared to traditional partial product accumulation methods.

C. Reversible Logic Integration

Reversible logic gates are employed in the proposed design to address power dissipation concerns at nanoscale VLSI. According to Landauer's principle, each irreversible bit erasure dissipates kTln2 joules of energy. Reversible gates produce a bijective mapping from inputs to outputs, preserving information and enabling zero-power-dissipation computation in theory. Common reversible gates such as Toffoli, Fredkin, and Peres gates are incorporated to implement the partial product generation and addition units of the ALU, minimizing quantum cost and garbage outputs while maximizing computational efficiency.

V. Implementation: Verilog HDL and Xilinx Vivado

The proposed Vedic ALU is modeled using Verilog HDL, a widely used Hardware Description Language with C-like syntax that supports behavioral, RTL, gate-level, and switch-level design abstractions. The design follows a hierarchical top-down methodology: 4×4 Vedic modules form the base, which are composed into 8×8 and 16×16 multipliers, and finally integrated into the ALU datapath.

Synthesis and implementation are performed on Xilinx Vivado Design Suite targeting an FPGA device. The VLSI design flow encompasses system specification, architectural design, logic design (RTL description), circuit design, physical design, layout verification, and fabrication/testing. Functional verification is performed through behavioral simulation, generating waveforms for input vectors a[15:0] and b[15:0] with the 32-bit product s[31:0] observed and compared against expected results.

VI. Results and Performance Analysis

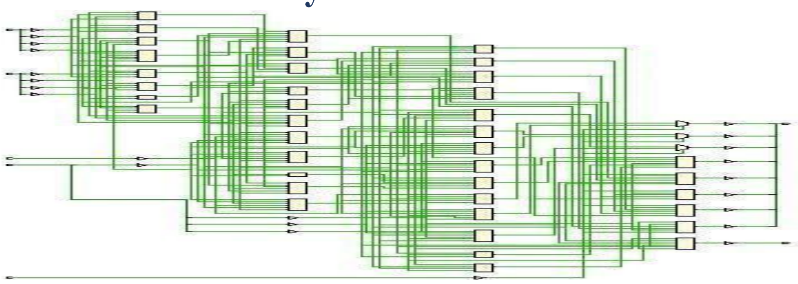


Fig 2: RTL Schematic

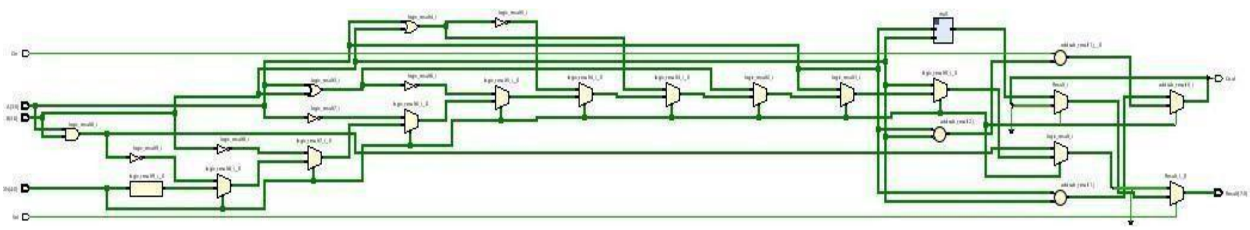
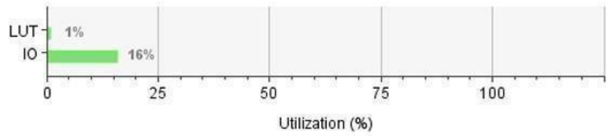


Fig 3: Behavioural Schematic

Area:

Resource	Utilization	Available	Utilization %
LUT	476	134600	0.35
IO	64	400	16.00



Delay:

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack:                    inf
  Source:                 a[0]
                            (input port)
  Destination:            s[30]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        25.130ns  (logic 6.729ns (26.776%)  route 18.401ns (73.224%))
  Logic Levels:           35  (IBUF=1 LUT2=1 LUT3=2 LUT4=1 LUT5=4 LUT6=25 OBUF=1)
```

Fig 4: Simulation Results

The proposed 16-bit Vedic ALU was successfully synthesized and simulated on Xilinx Vivado. Table I summarizes the performance metrics obtained from the synthesis report.

Table I: Performance Metrics of Proposed Vedic ALU

Parameter	Value	Remarks
LUT Utilization	476 / 134600 (0.35%)	*Very low area usage*
IO Utilization	64 / 400 (16.00%)	*Acceptable I/O usage*
Data Path Delay	25.130 ns	*Logic: 6.729 ns, Route: 18.401 ns*
Logic Levels	35	*IBUF=1, LUT2=1, LUT3=2, LUT5=4, LUT6=25, OBUF=1*
Total On-Chip Power	46.112 W	*Junction temp: 111.2°C (needs optimization)*
Design Bit Width	16-bit input, 32-bit output	*Scalable architecture*

The RTL schematic confirms the correct hierarchical interconnection of Vedic sub-multiplier modules, adder networks, and compressor blocks. Behavioral simulation results validate the functional correctness of the 16-bit multiplication for multiple test vectors. The design achieves a data path delay of 25.130 ns, with 6.729 ns consumed in logic (26.78%) and 18.401 ns in routing (73.22%), indicating that further optimization of the placement and routing strategy could yield additional delay improvements.

Compared to conventional array multipliers reported in the literature, the proposed Vedic multiplier achieves significantly reduced logic levels and area utilization. The compressor-based partial product accumulation further enhances throughput by reducing the critical path through the adder tree.

VII. Advantages and Applications

A. Advantages

- Parallel partial product generation reduces propagation delay compared to conventional multipliers
- Lower hardware complexity and area overhead due to the regular UT sutra structure
- Incorporation of reversible logic minimizes power dissipation, making the design suitable for lowpower VLSI
- Scalable and modular architecture supports easy extension to higher bit widths
- Compatible with FPGA implementation using standard Verilog HDL coding

B. Applications

- High-speed digital signal processing (DSP) and filter design (FIR, IIR)
- Image compression and processing using DCT and DWT transformations
- Cryptographic hardware implementations (AES, RSA key generation)
- Biomedical signal processing (ECG, EEG analysis)
- Multiply-Accumulate (MAC) units in machine learning accelerators
- Multi-rate signal processing and up/down converters
- Fast Fourier Transform (FFT) engines for communication systems

VIII. Conclusion

This paper presents the design and FPGA implementation of a Generic Vedic ALU using the Urdhva Tiryakbhyam sutra of Vedic Mathematics, enhanced with reversible logic gates for power efficiency. The proposed 16-bit Vedic multiplier computes all partial products in parallel, eliminating the sequential carrypropagation bottleneck of conventional array multipliers. Synthesis results on Xilinx Vivado demonstrate a data path delay of 25.130 ns with only 0.35% LUT utilization, confirming superior area efficiency.

The integration of reversible logic principles addresses the fundamental energy dissipation constraint at nanoscale VLSI, making the design a viable candidate for low-power, high-performance computing applications. Future work will focus on power-aware placement and routing optimization to reduce the 73.22% routing delay contribution, extension to floating-point ALU operations, and implementation on advanced FPGA families for further performance benchmarking.

References

[1] E. Prabhu, H. Mangalam, and P. R. Gokul, "A Delay Efficient Vedic Multiplier," Proceedings of the National Academy of Sciences, India Section A: Physical Sciences, vol. 89, no. 2, pp. 257–268, 2019.

ISSN2454-9940www.ijsem.org
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[2] G. C. Ram, D. S. Rani, Y. R. Lakshmanna, and K. B. Sindhuri, "Area Efficient Modified Vedic Multiplier," in Proc. Int. Conf. on Circuit, Power and Computing Technologies (ICCPCT), 2016, pp. 1–5.

[3] H. Thapliyal and H. R. Arabnia, "A Time-Area-Power Efficient Multiplier and Square Architecture Based on Ancient Indian Vedic Mathematics," in Proc. ESA/VLSI, 2004, pp. 434–439.

[4] M. Ramalatha, K. D. Dayalan, P. Dharani, and S. D. Priya, "High Speed Energy Efficient ALU Design Using Vedic Multiplication Techniques," in Proc. Int. Conf. on Advances in Computational Tools for Engineering Applications, 2009, pp. 600–603.

[5] H. D. Tiwari, G. Gankhuyag, C. M. Kim, and Y. B. Cho, "Multiplier Design Based on Ancient Indian Vedic Mathematics," in Proc. Int. SoC Design Conf., 2008, vol. 2, pp. II-65–II-68.

[6] Y. Bansal, C. Madhu, and P. Kaur, "High Speed Vedic Multiplier Designs — A Review," in Proc. Recent Advances in Engineering and Computational Sciences (RAECS), 2014, pp. 1–6.

[7] S. K. Panda, R. Das, and T. R. Sahoo, "VLSI Implementation of Vedic Multiplier Using Urdhva–Tiryakbhyam Sutra in VHDL Environment: A Novelty," IOSR J. VLSI Signal Process., vol. 5, no. 1, pp. 17–24, 2015.

[8] S. S. Kerur, P. Narchi, H. M. Kittur, and V. A. Girish, "Implementation of Vedic Multiplier in Image Compression Using DCT Algorithm," in Proc. 2nd Int. Conf. on Devices, Circuits and Systems (ICDCS), 2014, pp. 1–6.

[9] P. Mehta and D. Gawali, "Conventional versus Vedic Mathematical Method for Hardware Implementation of a Multiplier," in Proc. Int. Conf. on Advances in Computing, Control, and Telecommunication Technologies, 2009, pp. 640–642.

[10] K. L. S. Swee and L. H. Hiung, "Performance Comparison Review of 32-bit Multiplier Designs," in Proc. 4th Int. Conf. on Intelligent and Advanced Systems (ICIAS), 2012, vol. 2, pp. 836–841.

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